International Microwave and Optoelectronics Conference (IMOC) 2007
October 29 – November 1, 2007
Salvador, Bahia, Brasil

Half Day Tutorial Workshop

TITLE: Advanced Topics in RF MEMS

DATE: October 29, 2007

TIME: 2 – 6 PM

ORGANIZER: Sergio Pacheco, Freescale Semiconductor

DESCRIPTION: RF MEMS technology has rapidly evolved and matured over the last decade. More than 60 companies are currently involved in RF MEMS development with around 25% shipping commercial products or samples to customers. According to industry projections, by 2009, the RF MEMS market will break the $1 billion barrier. This workshop will present the latest advancements on the development of such RF MEMS devices and systems. Potential presentations will include discussions regarding the burgeoning RF MEMS market, issues in modeling and design of RF MEMS devices, the use of RF MEMS to facilitate reconfigurable systems, and how such systems will impact consumer/wireless electronics.

SPEAKERS / TOPICS:

- **Scott Barker** (University of Virginia, United States) – *Distributed MEMS Transmission Lines for Reconfigurable Circuits*
- **Marcelo Pisani** (University of Pennsylvania, United States) – *Piezoelectric RF MEMS Resonators, Filters and Switches*
- **Julio Costa** (RFMD, United States) – *RF-MEMS Wafer Level Packaging*
- **Robert Plana** (CNRS-LAAS, France) – *Multiphysics Issues in RF MEMS Modelling and Design*
- **Art Morris** (Wispry, United States) – *Multi-band and Multi-mode RF MEMS Architectures and Front-Ends*

Distributed MEMS Transmission Lines for Reconfigurable Circuits

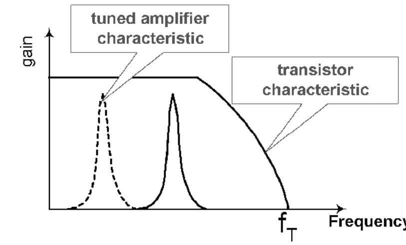
N. Scott Barker
University of Virginia
USA

International Microwave and Optoelectronics Conference

UNIVERSITY of VIRGINIA

Motivations

- Tuning microwave amplifier characteristics
- Highly integrated intelligent real time adaptable RF front-ends systems
- Highly integrated microwave/millimeter-wave circuits
- Reconfigurable wireless and satellite communication systems
- On wafer noise or load-pull measurement systems

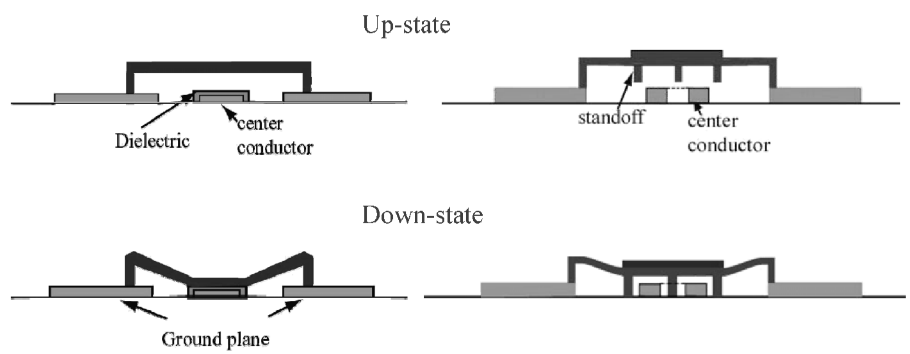


low loss, small size, very low power consumption and high linearity tunable matching network is needed

Outline

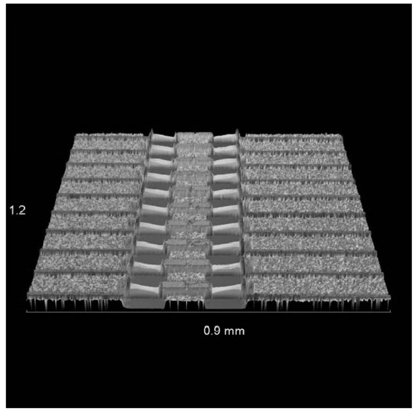
- Minimal contact RF-MEMS varactors
- Distributed MEMS transmission line (DMTL) tunable double-slug matching network-design
- DMTL tunable matching network-measurements
- Conclusions

Minimal Contact RF-MEMS Varactor



•Capacitance ratio can be controlled by the locations and the heights of the standoffs.

Mechanical Modeling

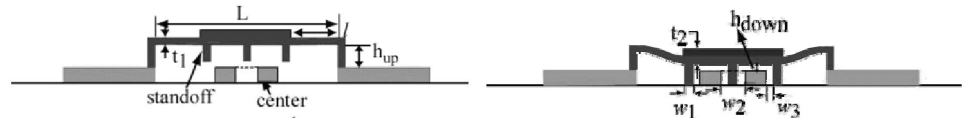


$$k = k_{bending} + k_{stretching}$$

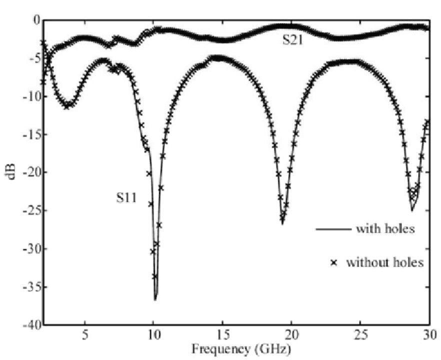
$$k = 2Ew\left(\frac{t}{l}\right)^3 + 2\frac{Ewt(\sqrt{h^2+l^2}-l)}{l\sqrt{h^2+l^2}} = 2Ew\left(\frac{t}{l}\right)^3 + Ewt\frac{(g_0-g)^2}{l^3}$$

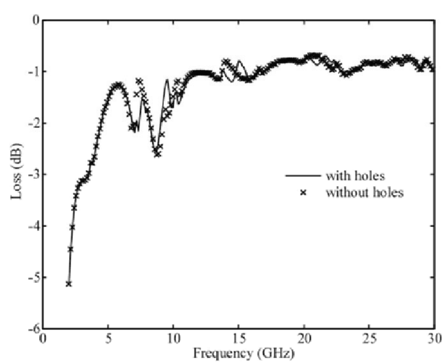
Fabricated design parameters

w	40 μm	L	300 μm
t_2	4 μm	t_1	0.5 μm
h_{up}	2.5 μm	h_{down}	0.4 μm
w_1	5 μm	w_2	25 μm
w_3	10 μm	l_2	77 μm



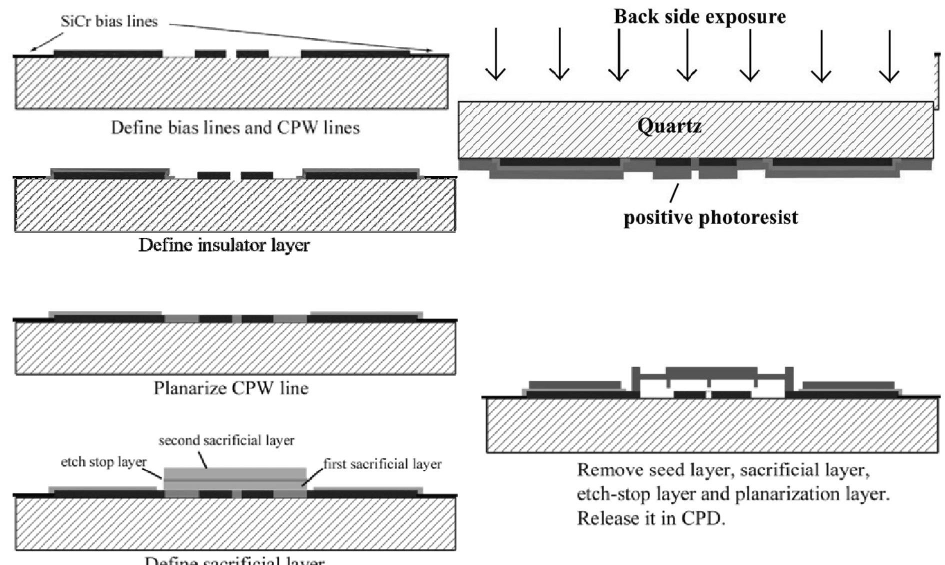
Center holes effects



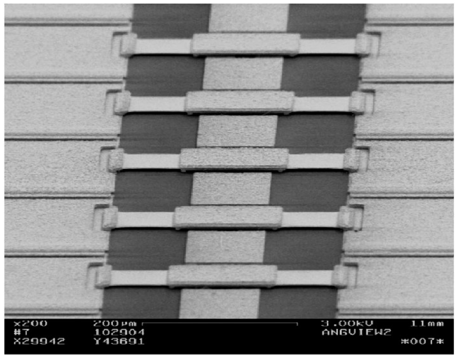


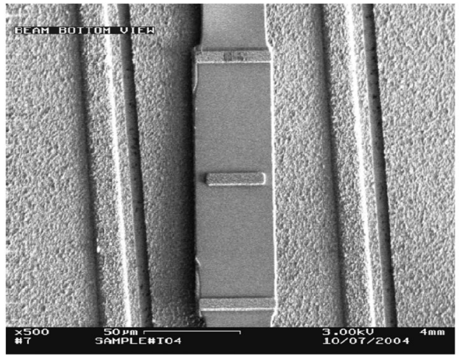
- Holes have no effect on line impedance or loss

Fabrication Process



SEM-Distributed Transmission Line





Outline

- Minimal contact RF-MEMS varactors
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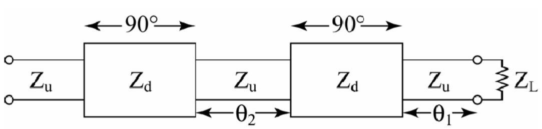
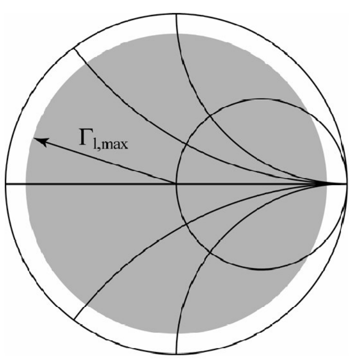
What is a Double-Slug Tuner?



$$VSWR_{max} = \left(\frac{Z_u}{Z_d}\right)^4$$



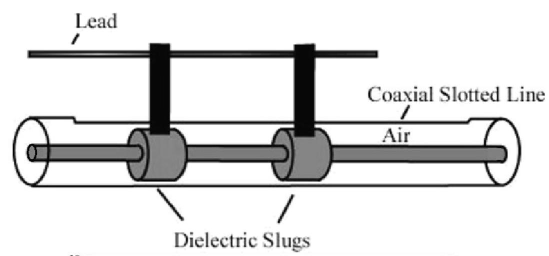
$$\left|\Gamma_{l,\max}\right| = \frac{VSWR_{\max} - 1}{VSWR_{\max} + 1}$$

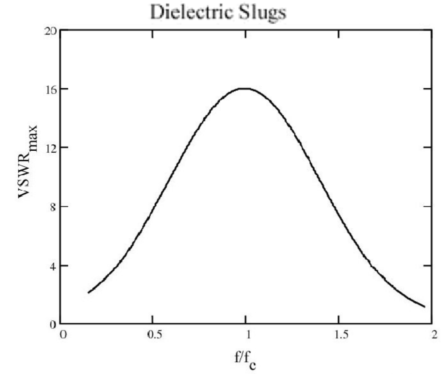
$$(\theta_1 + \theta_2)_{\max} = 270°$$

Z_u=50 Ω, Z_d=25 Ω ⇒ $VSWR_{max}$=16:1

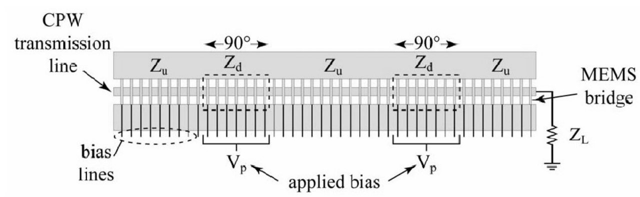
$\Gamma_{l,max}$=0.8824 ⇒ Z_L=3 to 800 Ω

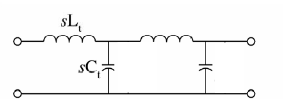
Limited Bandwidth for Fixed Length Slugs





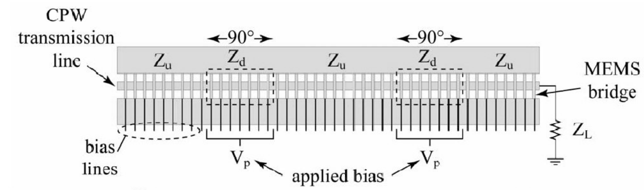
Distributed MEMS Transmission Lines

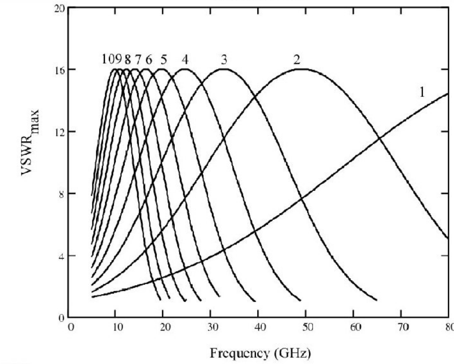




$$Z_o = \sqrt{\frac{L_t}{C_t}} \qquad Z = \sqrt{\frac{L_t}{C_t + C_b / s}} \qquad \upsilon = \frac{1}{\sqrt{L_t\left(C_t + C_b / s\right)}}$$

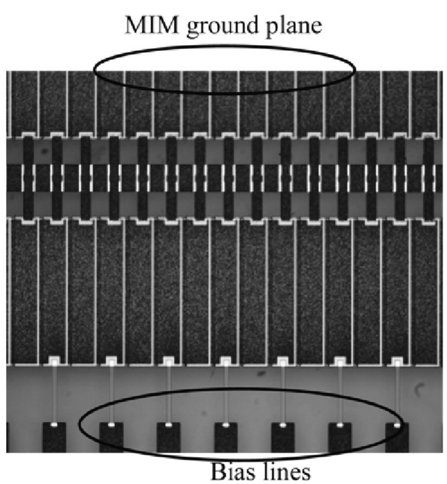
Tunable Length Slug – Broadband Operation



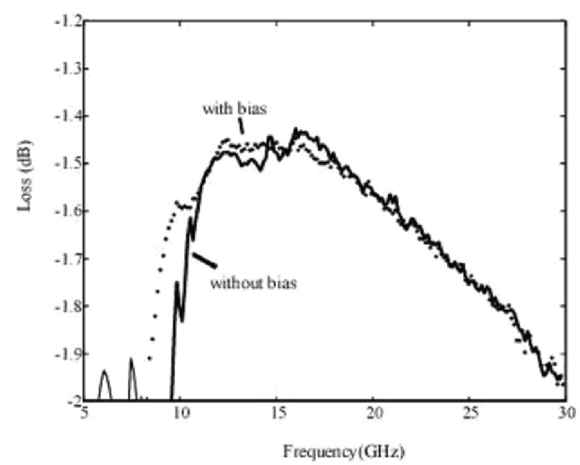


Biasing Scheme

- Implement Metal-Insulator-Metal (MIM) capacitors to separate DC bias lines and maintain RF ground plane.
- PECVD Si_xN_y is the insulator layer.
- Each MIM capacitor is designed at 15pF with 30pF for two in parallel to present a good short circuit above 5 GHz.



Bias lines loss



DMTL Double-Slug Tuner Design Equations

Beam spacing

$$s = \frac{1}{n_{90}}\left[\frac{1}{4}\left(\frac{\lambda_o}{\sqrt{\varepsilon_{r,eff}}}\frac{Z_d}{Z_o}\right)\right]$$

λ
low-impedance section

Total # of beams

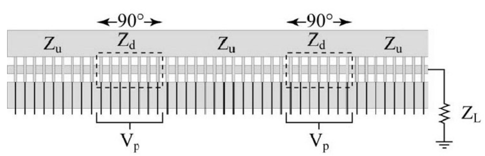
$$N = n_{90}\left(3\frac{Z_u}{Z_d}+2\right)$$

Total length

$$l = s \cdot N$$

Capacitance ratio

$$C_r = \frac{\frac{1}{Z_d^2}-\frac{1}{Z_o^2}}{\frac{1}{Z_u^2}-\frac{1}{Z_o^2}}$$



Fabricated Design Parameters

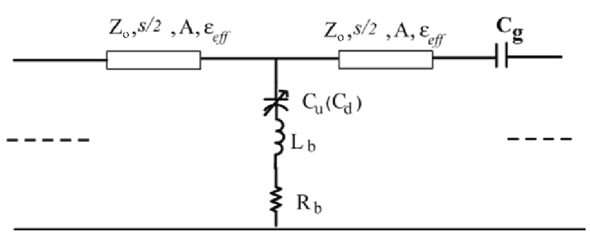
CPW Parameters

substrate	quartz (ε_r = 3.78)
dimensions	100/100/100 µm
Z_o	96 Ω
$\varepsilon_{r,eff}$	2.39

Double-Slug Design

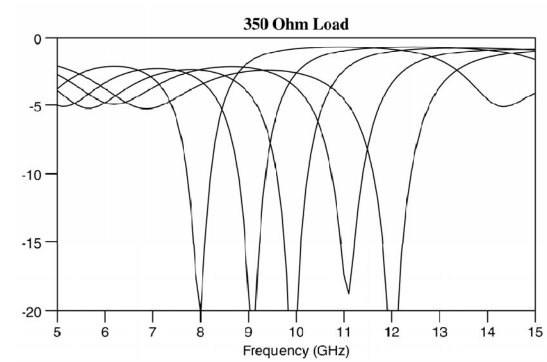
design frequency	10 GHz	# of beams in 90°	10
Total # of beams	80	beam spacing (*s*)	126 µm
C_{bu}	18 fF	Z_u	50 Ω
C_{bd}	87 fF	Z_d	25.6 Ω
C_r	4.8	$VSWR_{max}$	14.4

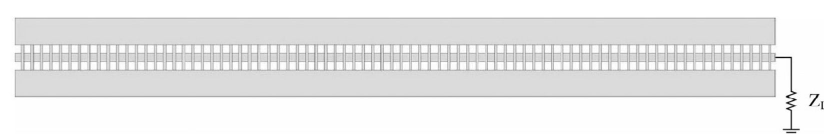
DMTL Circuit Model



- Z_o is the unloaded impedance
- L_b and R_b are the bridge inductance and resistance.
- C_d is the MEMS bridge capacitance when it is in the down state, and C_u is the up-state MEMS bridge capacitance.
- s is the switch spacing and A is attenuation of the unloaded line.

Linear Simulation of DMTL Tuner





Outline

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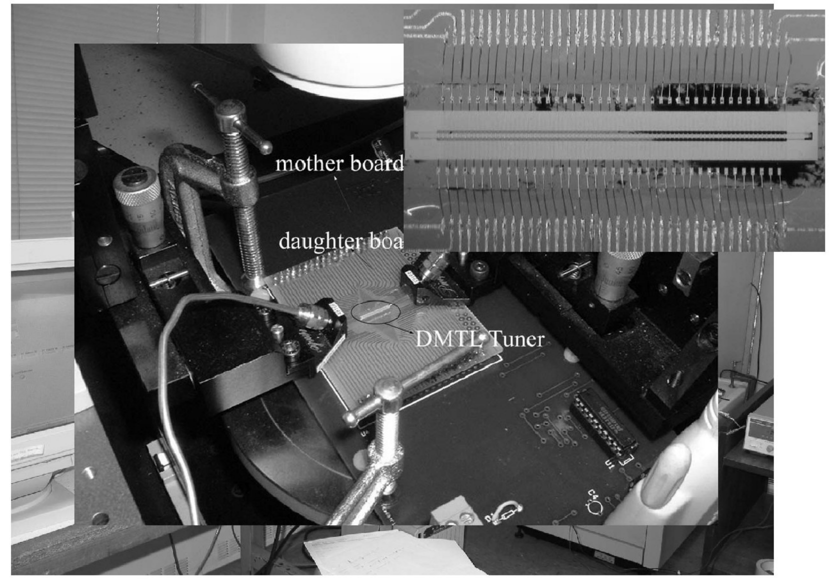
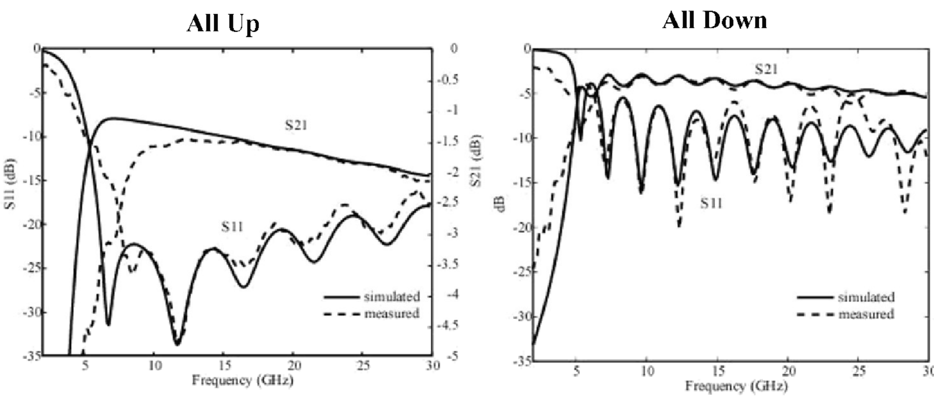
Measurement setup

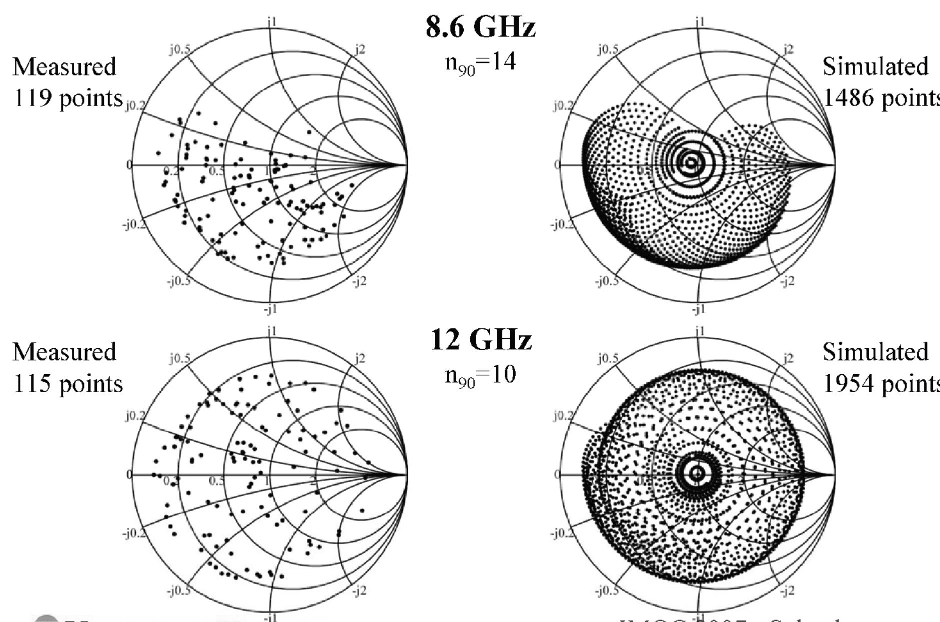


Capacitance Ratio Measurements



Equivalent circuit fitted parameters	C_u	C_d	C_r	L_b	R_b	A @ 20GHz	C_g
	16 fF	78 fF	4.9	15 pF	0.1 Ω	0.85 dB/cm	20 pF

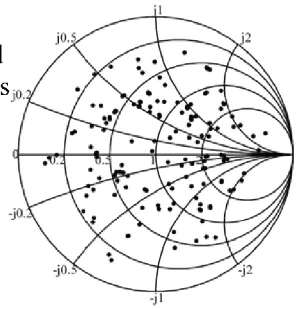
Impedance coverage – Measurement & Simulation



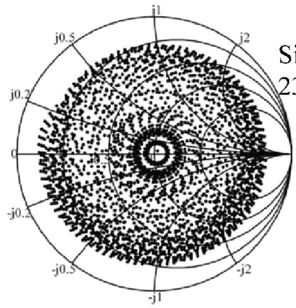
Impedance coverage cont.

20 GHz
n_{90}=4

Measured
160 points

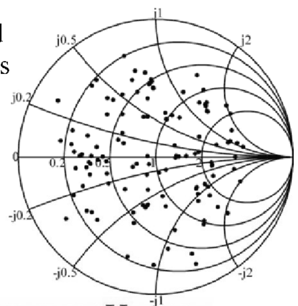


Simulated
2347 points

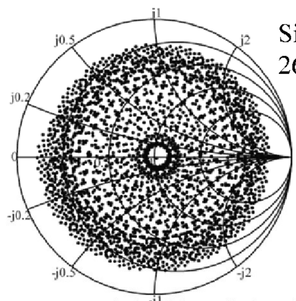


27.8 GHz
n_{90}=3

Measured
126 points

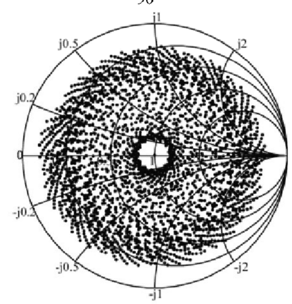


Simulated
2629 points

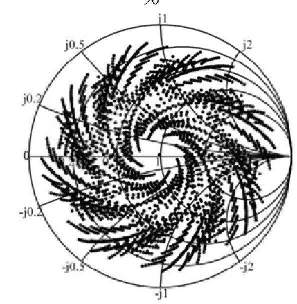


Impedance coverage cont. (simulation only)

30 GHz
n_{90}=3



50 GHz
n_{90}=2



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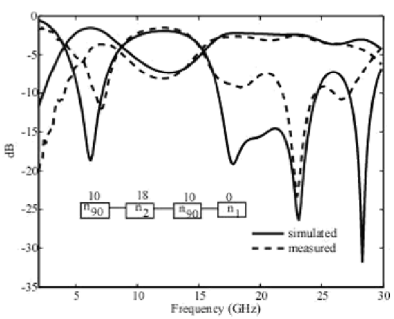
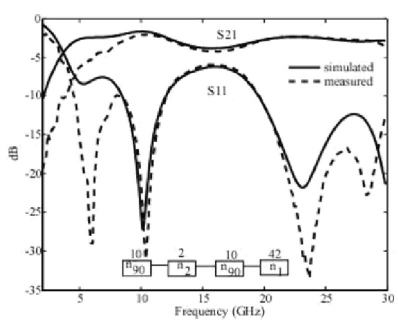
Measured DMTL tuner loss

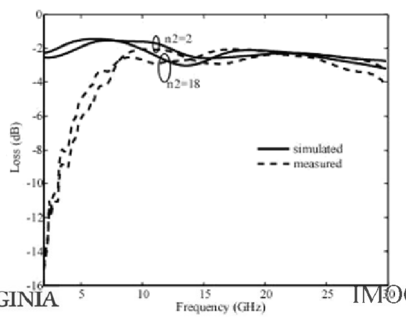




VSWR=12:1

VSWR=2:1

fc=12 GHz



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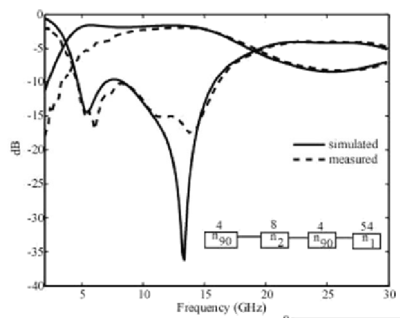
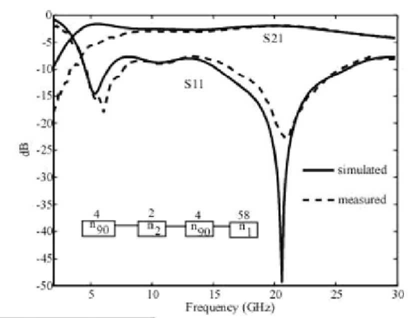
Measured DMTL tuner loss

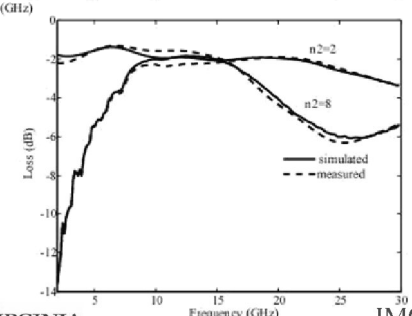




VSWR=5:1

VSWR=2:1

fc=24 GHz



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Conclusions

- Development of a novel minimal contact RF-MEMS varactor
  - Capacitance ratio control and measured C_r=2.5~5
  - No intimate contact between dielectric layer and RF-MEMS beam resulting in no charging and reduced stiction
  - Development of accurate fabrication process for defining standoffs
- Development of DMTL tunable matching network
  - Low loss biasing design
  - Very uniform coverage of Smith Chart over a broad operation bandwidth extending from 10 GHz to 50 GHz
  - Tradeoffs for loss and instantaneous bandwidth
  - Very good performance of the fabricated device measured from 8-30GHz

Piezoelectric RF MEMS Resonators, Filters and Switches

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Penn University of Pennsylvania

Outline

- Motivation
- Piezoelectric AlN Technology Overview
- AlN Contour-Mode Resonators
- AlN Contour-Mode Filters
- Piezo-actuated RF Switches
- MEMS-Based RF Front-Ends
- Conclusions

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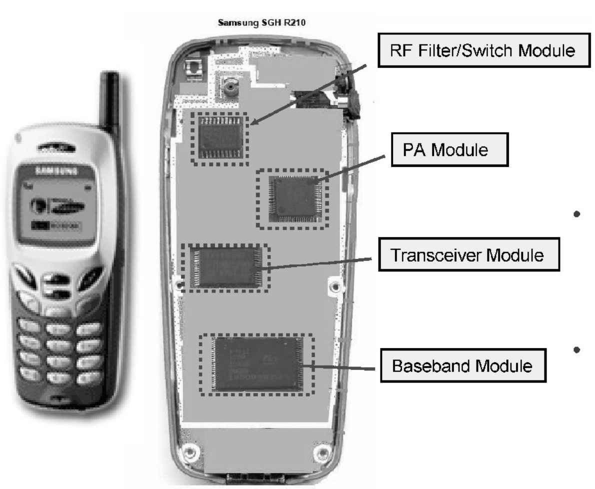
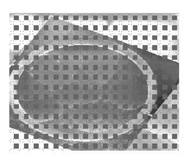
Next Generation Integrated RF Modules





- **Novel RF MEMS** technology will enable compact integrated RF Modules and transceivers
- **Key advantages:** reduced components count, free up space for new applications, lower power consumption and lower costs

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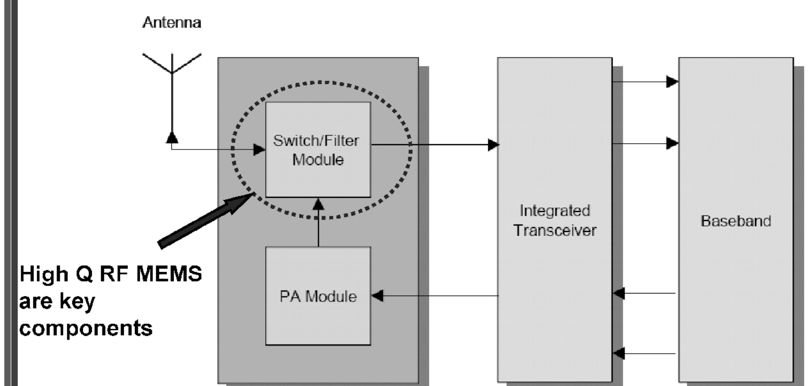
Modular Integration of Components



- Discrete components will be co-integrated with transistors: area, cost and power savings, gains in functionality (batch fabrication and availability of arrays of small high-Q passives)

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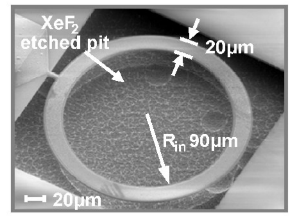
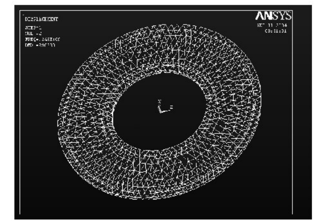
Piezoelectric AlN RF-MEMS Technology Overview

Technology Overview

- **Piezoelectric AlN films** available in production environments (state of the art DC sputtering tools)
- Use of **contour-mode** resonators permits the fabrication of arrays of piezoelectric microresonators with **different frequencies on a single chip**
- Demonstrated **low motional resistance** that enables direct interface with 50 Ω systems



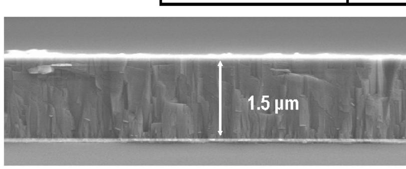


AlN Film Properties

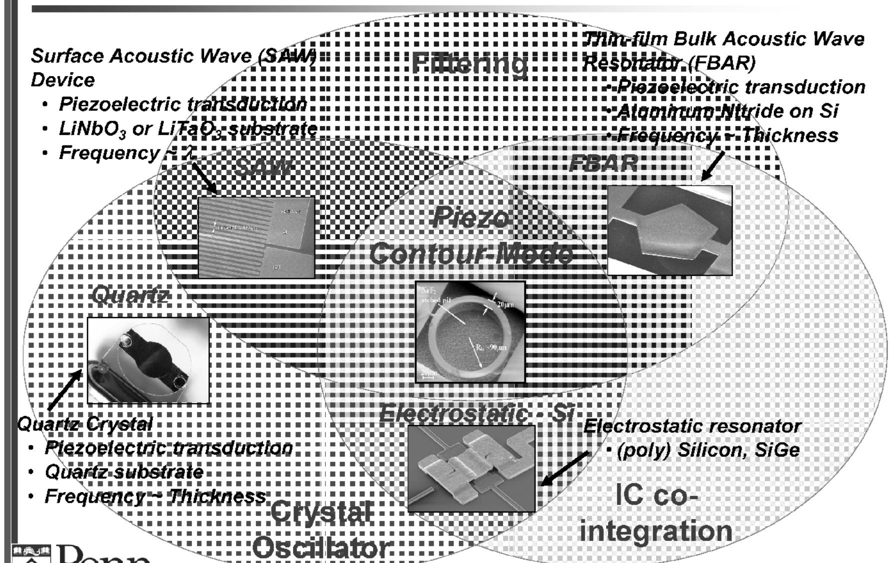
Optimal Properties of AlN:

- Very high sound velocity
- Very low permittivity
- High Resistivity
- Good dielectric strength
- Compatibility with IC manufacturing

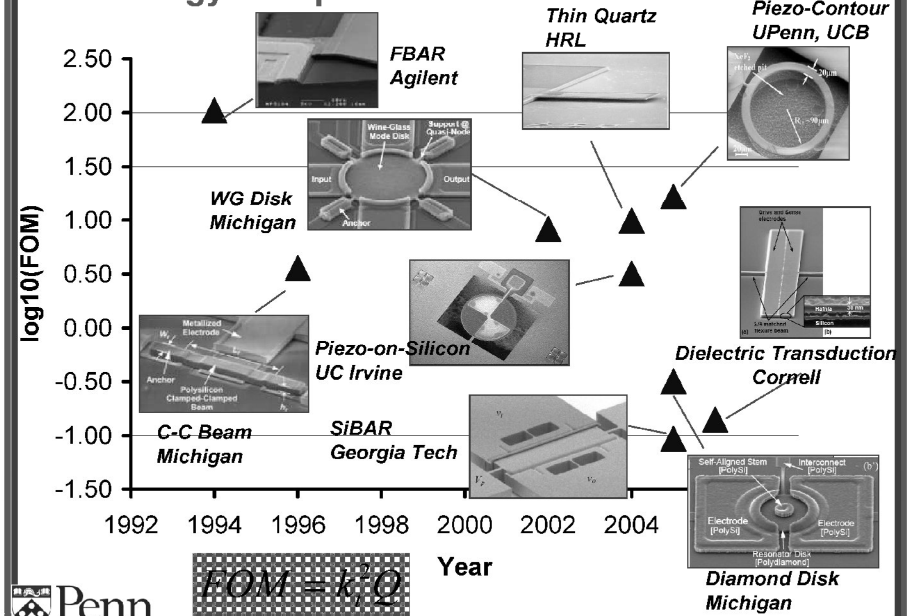
Property	AlN	ZnO	PZT
Sound Velocity ([km/s])	11.4	5.35	4.5
Piezo coefficient (d_{31}) [pC/N])	~2	~4	~100
Permittivity (ε_3)	9	10	~1000
Resistivity ([Ωcm])	10^{13}	10^{7}	10^{9}
Dielectric Strengthness ([kV/mm])	20	10	100
K_{t31}^2 [%]	2.5	2.5	8-12



Technology Comparison



Technology Comparison



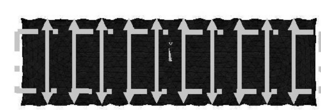
AlN Contour-Mode Resonators

VHF and UHF Resonators

- Contour-mode resonators in the VHF and UHF range are the basic building blocks that will enable the co-fabrication of oscillators and filters in a single chip
- Design Goals:
  - Multiple frequencies on same wafer
  - Small R_x
  - Small size
  - High-Q
  - Co-design with switches and other passives: piezo-based RF-MEMS technology platform

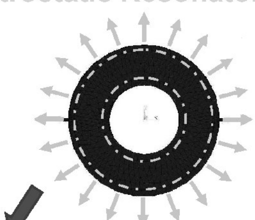
State-of-the-art RF MEMS Resonators

FBAR Resonators



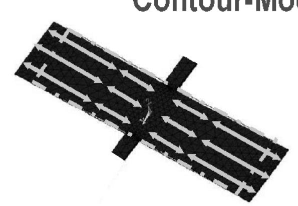
<R. Ruby, IEEE Ultrasonic Symp '03>

Electrostatic Resonators



<S.-S. Li, MEMS '04>

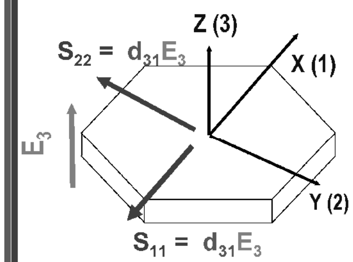
Contour-Mode AlN Resonators of this Work



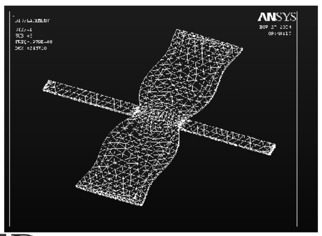
- Contour-mode → multiple frequencies
- Body forces → large η and small R_x
- Relatively High-Q

G. Piazza et. al, "Single-Chip Multiple-Frequency Filters Based on Contour-Mode Aluminum Nitride Piezoelectric Micromechanical Resonators", Proc. of Transducer's 2005.

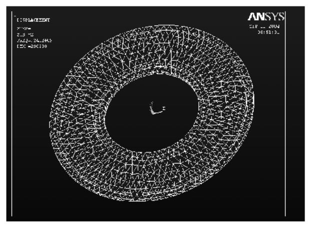
Resonator Design



- Contour mode of vibration induced via d_{31} piezoelectric coefficient
- Main geometries: rings and rectangular plates
- One dimension sets the frequency whereas second dimension is used to set the reactance value



$$f_o \approx \frac{1}{2W} V_p$$



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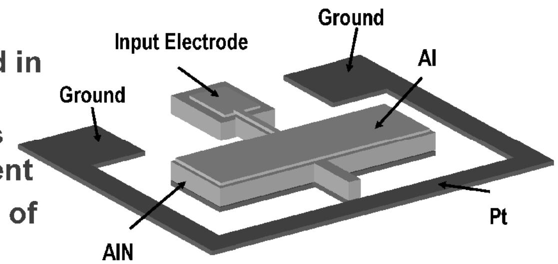
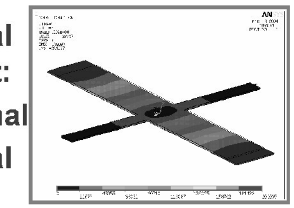
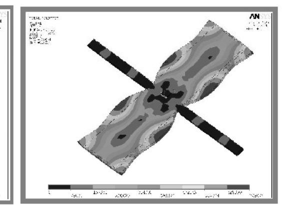
Rectangular Plates

- In-plane contour modes are excited in thin-film AlN rectangular plates using d_{31} coefficient
- Entire top surface of resonator is the electrode
- Only 2 fundamental modes are present:
  - Length Extensional
  - Width Extensional







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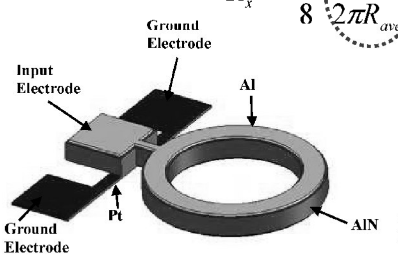
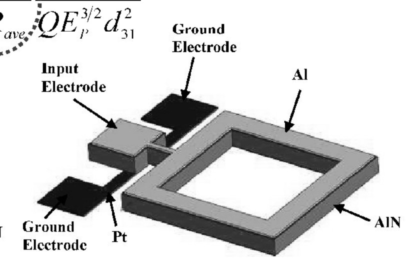
Contour-Mode AlN Ring Resonators

- Ring design extends frequency range providing for low motional resistance and high quality factors
- Frequency is set by the width of the ring
- Arbitrary selection of the value of motional resistance via the choice of the lateral area of the ring (range of 50 – 300 Ω)

$$R_x \approx \frac{\pi^2}{8} \frac{T}{2\pi R_{ave}} \frac{\sqrt{\rho}}{Q E_P^{3/2} d_{31}^2}$$





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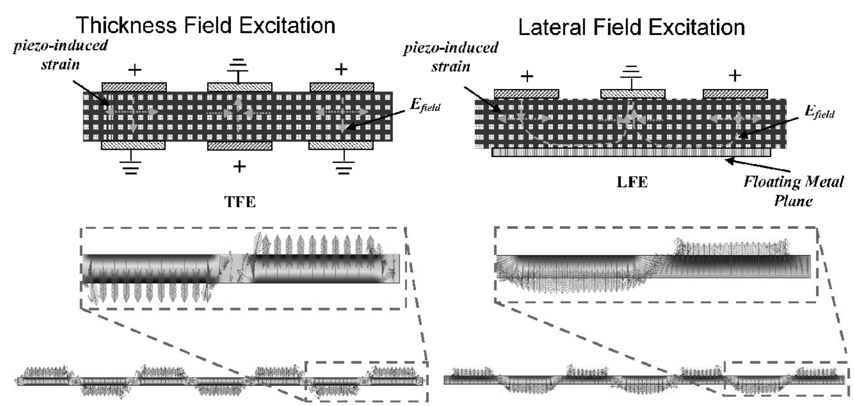
G. Piazza et. al, "Piezoelectric Aluminum Nitride Vibrating Contour-Mode MEMS Resonators", J. of MEMS, 15(6), 2006.

Higher Order Contour-Mode Resonators

- TFE and LFE excitation



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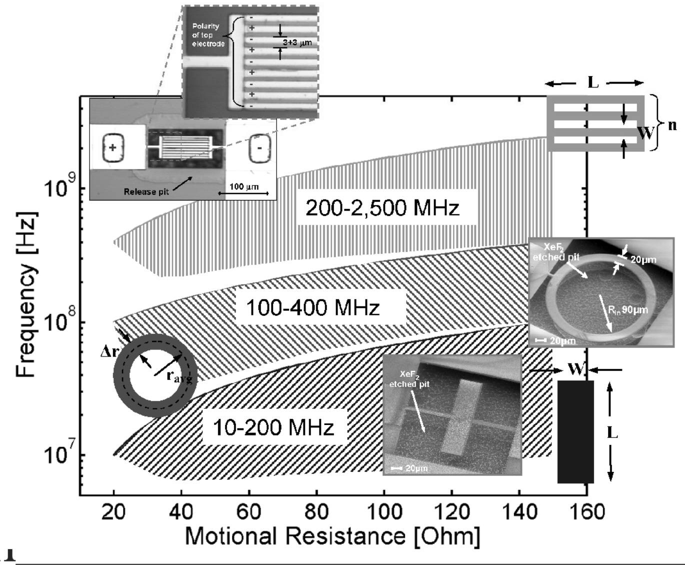
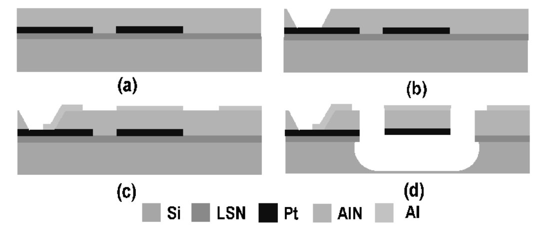
Resonator Geometry and Design Space



Fabrication Process



(a) LPCVD deposition of LSN, Pt patterning by lift-off and AlN sputter deposition

(b) Open contact by wet etch in H3PO4

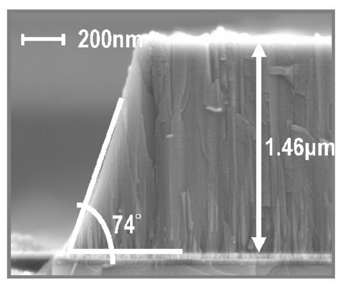
(c) Deposition of top Al electrode and dry etch in Cl2

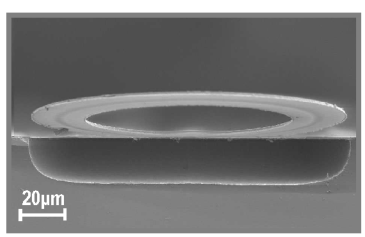
(d) Cl_2-based dry etching of AlN resonant structure and dry release in XeF_2

- 4-mask, potentially post-CMOS compatible (T_{max}< 400 ℃) fabrication process
- LSN used for improved isolation; patterning of bottom Pt electrode reduces parasitics
- AlN is anisotropically etched in Cl_2-based plasma
- Novel isotropic XeF2-based Si etch release AlN structures

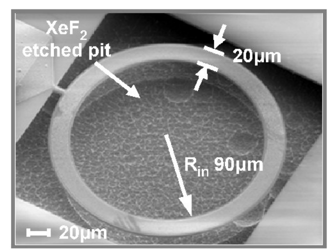
Aluminum Nitride Processing

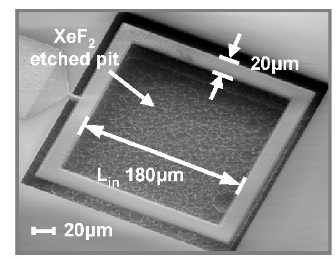
- Cl_2-based dry etching yields fairly straight sidewalls
- Hard mask is made out of LTO deposited on top of Al / Pt layer protected
- Etch rate depends on degree of crystallinity of AlN (~150 nm/min). Oxide etch rate is about 60 nm/min
- XeF_2 release selectively removes LSN and Silicon without attacking the resonator body



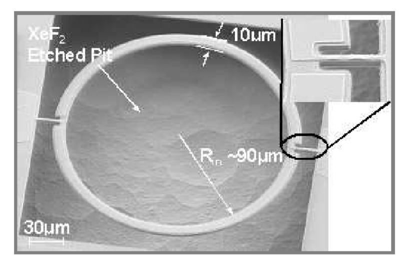


Fabricated Devices

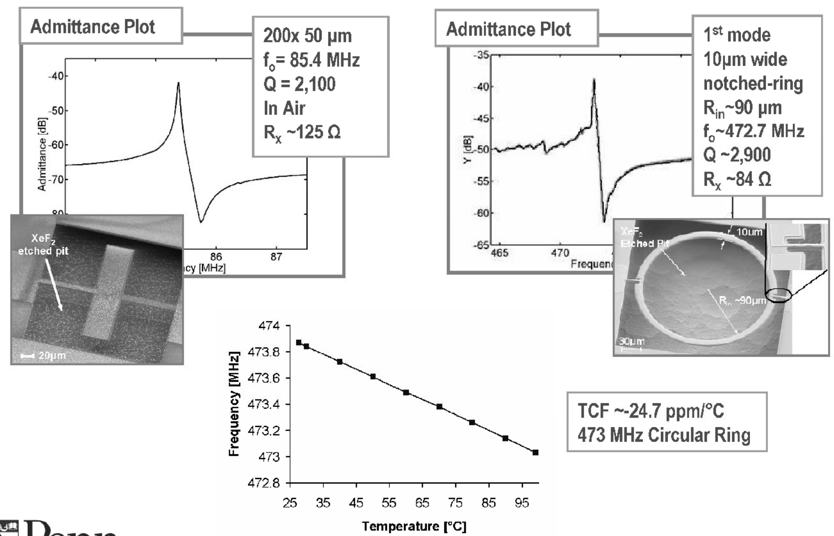




- Circular rings with average diameter of ~200 µm are suspended in air by 3 to 20 µm wide anchors
- Planar structures: Stress in AlN films is controlled to be below 200 MPa



Resonator Performance



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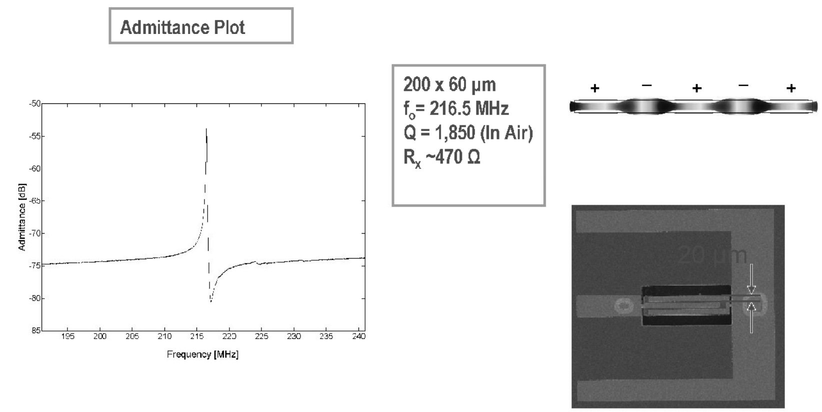
Resonator Performance

- Lateral Field Excitation at 216 MHz



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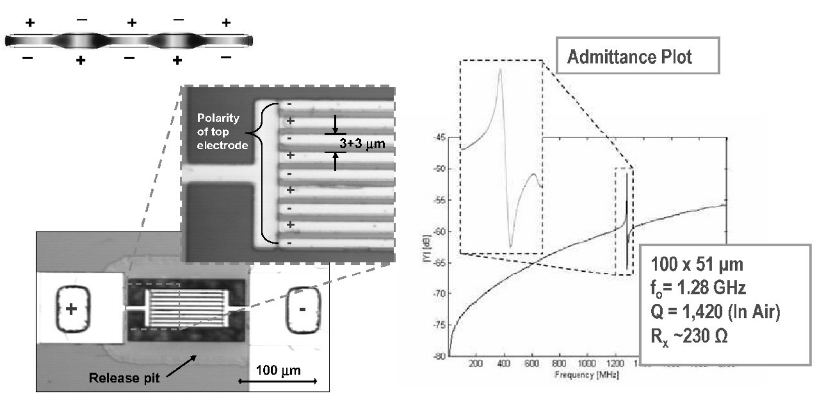
Resonator Performance



- New design improves fabrication tolerances and increases device stiffness

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Key Advantages

- Frequency is set by lithography step:
  - Multiple frequencies on the same silicon substrate
  - 10 x less sensitive to thickness variations than FBARs
  - High accuracy/yield (1,000 ppm) can be achieved lithographically up to 4 GHz
- High Q in air
- Matching to 50 Ω possible

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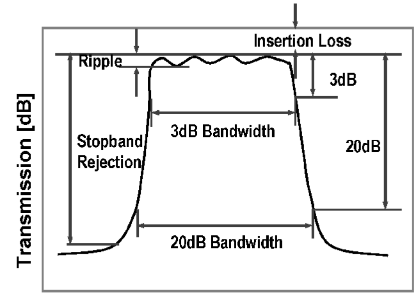
Contour-Mode Resonator Based IF and RF Filters

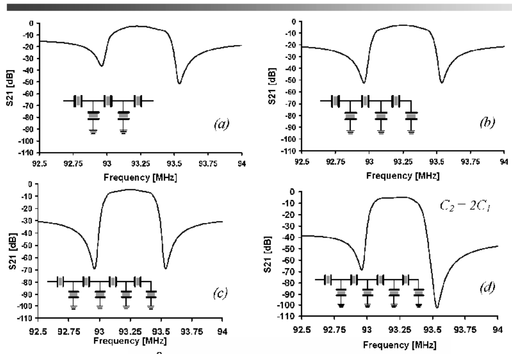
Filter Specifications

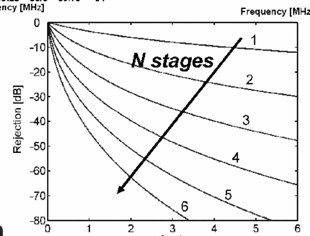
- Low insertion loss and interface to 50 Ω systems require high Q and low R_M
- BW depends on application and can vary from 0.3 - 2 MHz for IF filter to 50 MHz for RF Filters. We have demonstrated that resonators can cover IF BW, tough to go to GHz…unless new **DESIGNS** or **ARCHITECTURES** can be implemented
- Shape Factor depends on number of cascaded resonators and requires a high-yield and highly repeatable fabrication process



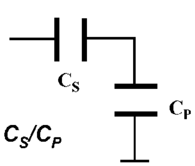
$$\text{20dB Shape Factor} = \frac{\text{20dB Bandwidth}}{\text{3dB Bandwidth}}$$

Ladder Filter Performance





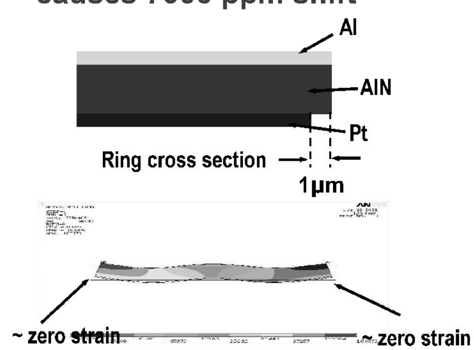
- Increase in IL with # of stages
- Increase out-of-band rejection with # of stages
- Improve shape factor with # of stages
- Cap ratio to set out-of-band rejection

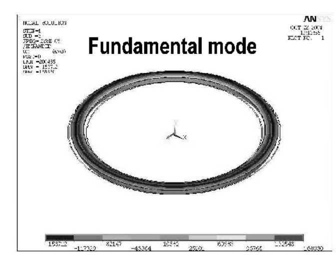


$C_{ratio} = C_S/C_P$

Process-Defined Frequency Shift

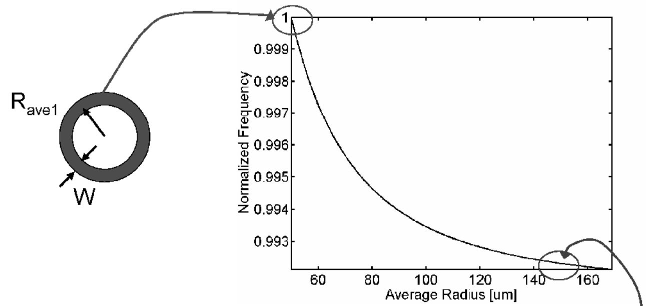
- Pt mass (6.5 x AlN density) loads resonator and shift its center frequency
- For a 100 μm radius ring, removing 1 μm of Pt causes 7000 ppm shift



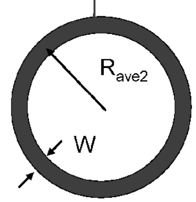


ANSYS f_o= 228 MHz
Experimental f_o=230 MHz

Geometry-Defined Frequency Shift

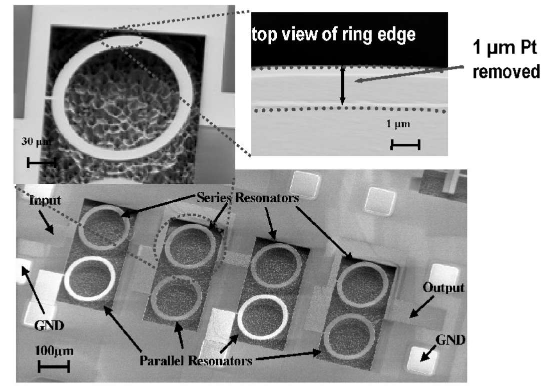


- Average radius of ring can be used to induce slight frequency shift
- ~ 0.7% shift by changing radius from 50 to 150 µm



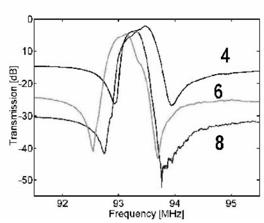
Filter Fabrication

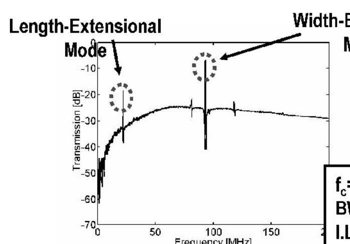
- Fabrication process uses the same 4-mask low temperature process
- Frequency shift is introduced by lithographically removing Pt from the series branch



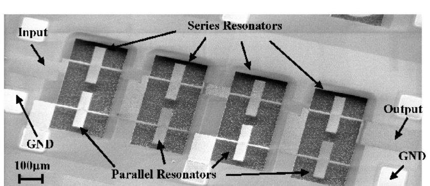
Ladder Filters with Rectangular Plates

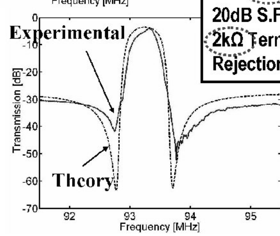
- Ladder structures with 4, 6 and 8 resonators have been demonstrated



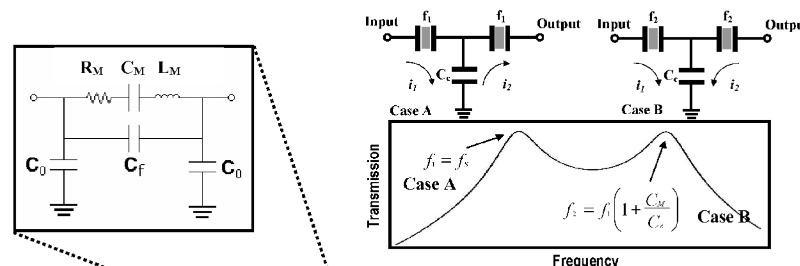


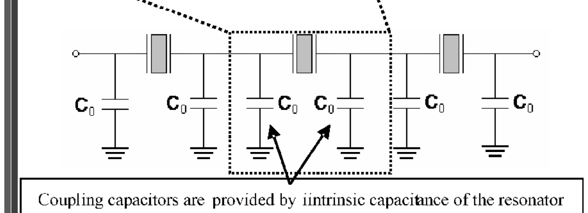
f_c=93.2 MHz
BW_{3dB}=305 kHz
I.L.= 4 dB
20dB S.F.= 2.2
2kΩ Termination
Rejection 27 dB





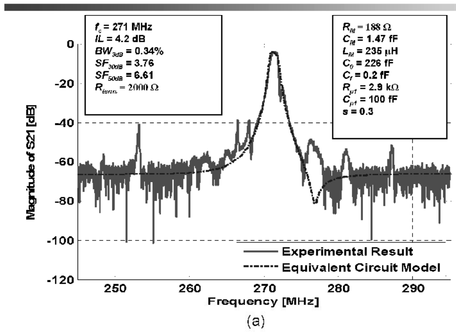
Self Cap-Coupled Filters

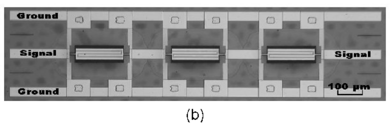




- No need for external caps (high Q)
- No need to shift center frequency (higher yield)
- Large rejection

Self-Cap Coupled Filters





Electrically coupled 3rd order filter:

- 271 MHz central frequency
- 0.35 % BW
- 4.2 dB insertion loss
- 2 kΩ motional resistance

(a) Transmission response and (b) Picture of a 271 MHz 3rd order AlN contour-mode filter.

C. Zuo et. Al, "Channel-Select RF MEMS Filters Based On Self-Coupled AlN Contour-Mode Piezoelectric Resonators", Proc. Of 2007 IEEE Ultrasonics Conference.

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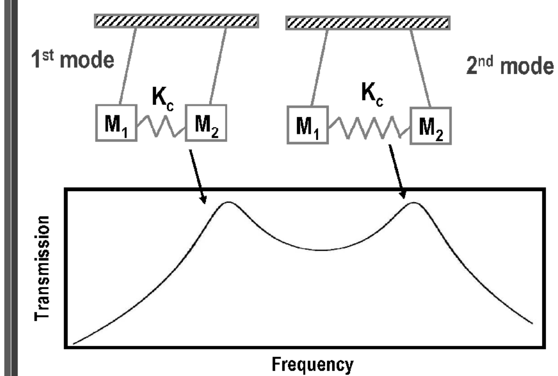
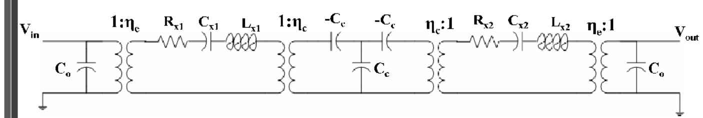
Mechanically Coupled Filters



Performance	Factor
Insertion Loss	Q, K_t^2 and filter order
Rejection	Parasitic
Shape Factor	Filter Order
Termination	Reactance
Bandwidth	Coupling Beam, Resonator Mass



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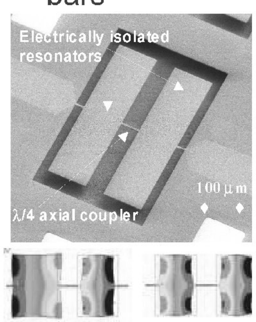
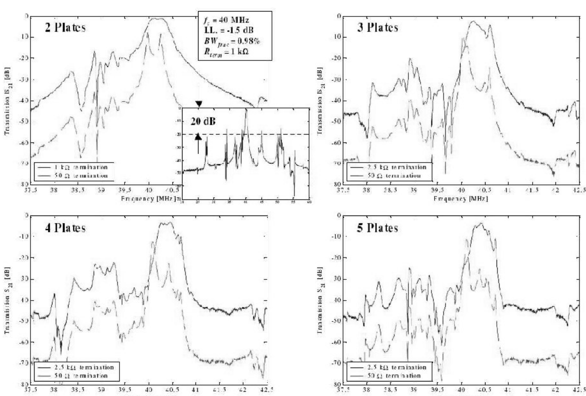
Mechanically Coupled Arrays

- Mechanically coupled filters from 2 to 5 plates have been fabricated and tested
- Coupling is achieved with 1 or 3 quarter-wavelength long bars





P.J. Stephanou, G. Piazza et. al, "Mechanically Coupled Contour Mode Piezoelectric Aluminum Nitride MEMS Filters", Proc. of MEMS'06.

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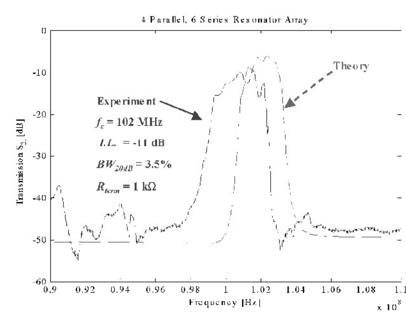
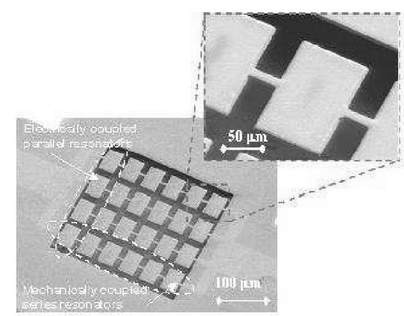
Hybrid Arrays

- Use arrays (electrically in parallel) of mechanically coupled resonators to increase filter order while maintaining small size and reducing matching impedance





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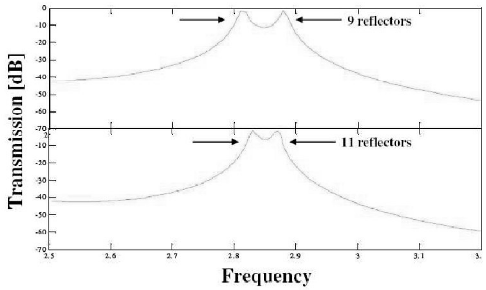
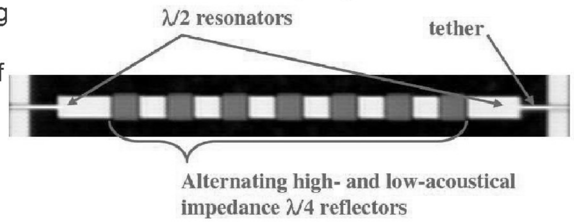
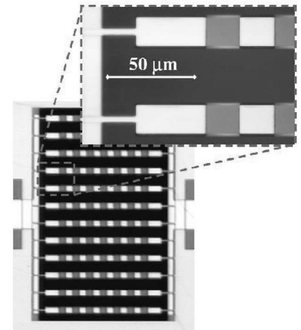
Monolithic Filters

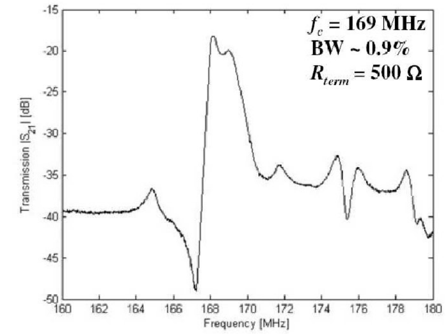
- Alternating layers of high and low acoustical impedance are used to set the filter bandwidth
- High and low acoustic impedance layers are realized by simply depositing thick Pt on AlN, therefore lowering the intrinsically high acoustic impedance of AlN





Monolithic Filters



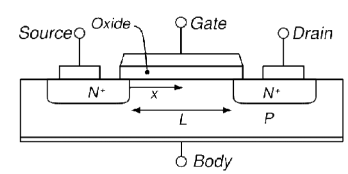


- Initial results for 6 alternating hi / low pairs are promising, but further development is required (e.g. better transducer layout)

Piezo-electric RF MEMS Switches

RF MEMS Switches

- Advantages over Solid State Switches
  - Improved Power Handling
  - Improved Isolation and Insertion Losses
  - Enabling new functionality by batch fabrication and co-integration with micromechanical resonators and filters
- Issues of Mechanical Devices
  - Reliability
  - Response time
  - Interface with low-voltage, low-power CMOS circuits
  - CMOS-process compatibility



Actuation Mechanisms

	Electrostatic	Piezoelectric	Thermal	Magnetic
Actuation Voltage (V)	20 – 80	3 – 20	3 – 5	3 – 5
Switching Time (μs)	1 – 200	5 – 500	300 – 10000	300 – 1000
Static Power (mW)	0	0	0 – 250	0 – 100

Desirable switch features:

- High Forces (> 100 μN)
- High Stiffness(> 100 N/m)
- Low Actuation Voltage (< 10 V)
- High Reliability (>10^8 – 10^{12} cycles)
- Simple and robust fabrication process: clean release process, reliable contact, compatibility with CMOS fabrication

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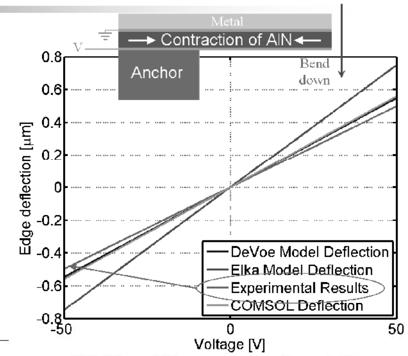
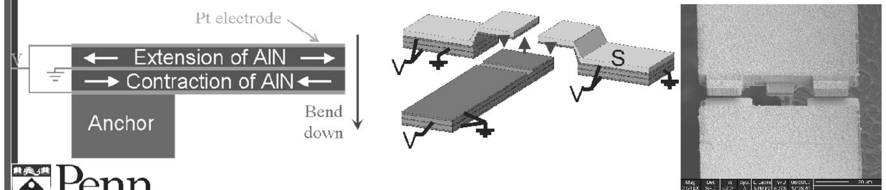
Piezo Actuated Switches

- Principle of bi-morph actuation validated by both analytical modeling and FEM simulations
- Deflections in the order of 0.5 μm for a single actuator demonstrated
- Dual actuation will double force, displacement and automatically provides self-stress-compensated structure
- Use the same technological platform of resonators and filters



Width = 50 μm, Length = 100 μm



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MEMS-Based RF Front-Ends: A Microsystems Approach

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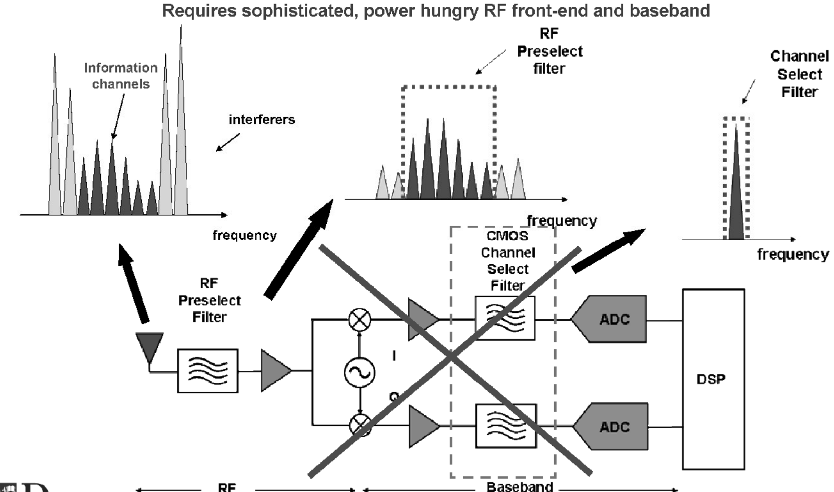
Sub-Sampling RF Channel Select Receiver

Legacy Direct Conversion Receiver

Requires sophisticated, power hungry RF front-end and baseband



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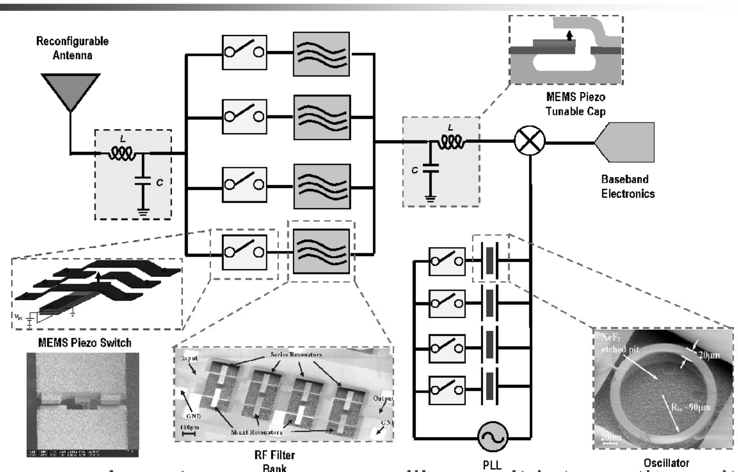
Single-Chip RF Module



- Low-temp process will permit integration with electronics and ultimately enable single-module radios and simpler architecture

Conclusions

- Introduced a new class of piezoelectric contour-mode vibrating MEMS
- Demonstrated high Q and low motional resistance resonators up to GHz
- Demonstrated Oscillators based on contour-mode devices
- Demonstrated Electrically and Mechanically Coupled Filters
- Switch actuation and design in good progress: demonstrated actuation
- All piezo-based RF-MEMS platform and signal processor

Future Research Directions

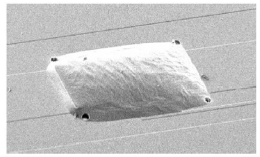
- Understanding of Ultimate Loss Mechanisms and Improvement of Resonator Q (Q > 5,000 expected)
- Temperature compensation (From -25 ppm/℃ Down to -0.25 ppm/℃)
- Direct Matching to 50 Ω RF Systems
- Co-Integration with CMOS and Packaging
- Design and Fabrication of RF Micromechanical Processors

Acknowledgements

- Funding Agencies:
  - DARPA / MTO (ASP, S&T)
  - NSF / NBIC
  - IBM, Nortel
- Research Group:
  - Prof. Gianluca Piazza, Dr. Rashed Mahameed
  - PhD Students: Nipun Sinha, Chengjie Zuo, Carlos Perez
- University of California Berkeley (BSAC, Prof. Albert Pisano)
- Tegal Corporation
- Harmonic Devices, Inc. (Philip Stephanou and Justin Black)

Thank you for your attention!

- Penn Micro and Nanosystems Group: http://www.seas.upenn.edu/~piazza



RF-MEMS WAFER LEVEL PACKAGING

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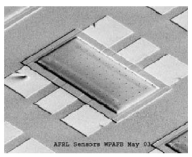
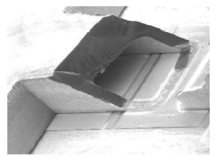
jcosta@rfmd.com

RFMD™

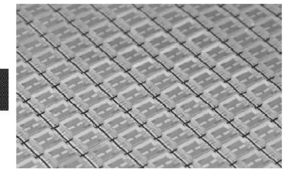


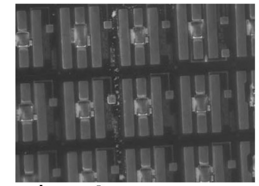


First, let's define WLP

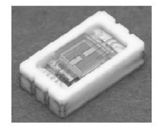
- WAFER LEVEL PACKAGING (WLP)
  - Refers to a packaging approach where all of the MEMS devices on the wafer are sealed / packaged AT THE SAME TIME, and then singulated into individual units.

OMRON





- Traditional (non-WLP) MEMS packaging approaches:

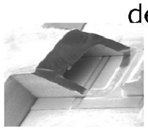


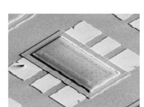
CERAMIC PACKAGES

INDIVIDUAL LID BONDING

INTRODUCTION

- Why Wafer-Level-Packaging?
  - Packaging of a MEMS device : allows for assembly of MEMS, guarantees specs/lifetime of MEMS component.
  - MEMS Devices such as RF switches / resonators MUST be encapsulated in hermetic or near-hermetic conditions. Specs/lifetime determine HOW hermetic.
  - Hermetic : means that moisture/atmosphere will not penetrate package and that environment inside package will not degrade or leak out.
  - Easiest approach is to seal in ceramic package under a controlled atmosphere. Problem: VERY EXPENSIVE!
  - Wafer-Level-Packaging (WLP) is inexpensive but DIFFICULT! It is often as hard or harder than making the MEMS device itself. Don't forget this!
  - Packaging needs to be engineered DURING the development of MEMS technology, not after.

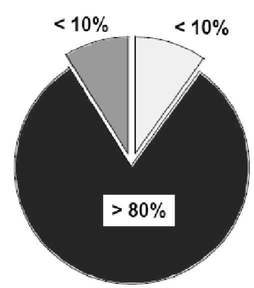




Switch Packaging Approaches
(Known Efforts)

Conventional (Chip-in-box) (<10%)
Dice ⇒ release ⇒ package or
Dice ⇒ package ⇒ release
Ceramic / Metal package

Thin-film Encapsulation (<10%)
Thin-film bubble, cap ⇒
Release through holes ⇒
Seal ⇒ Dice

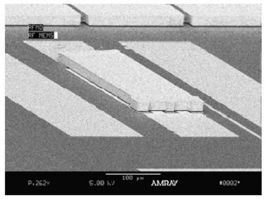


Approaches

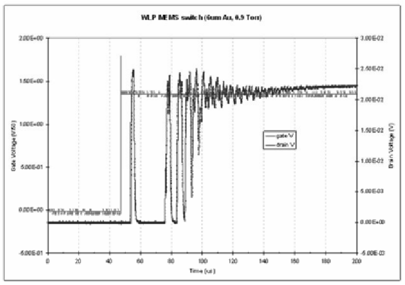
Wafer Bonding (> 80%)
Release ⇒
Bond cap wafer ⇒ Dice
Metal eutectic or Glass frit seal

RF-MEMS Packaging Requirements

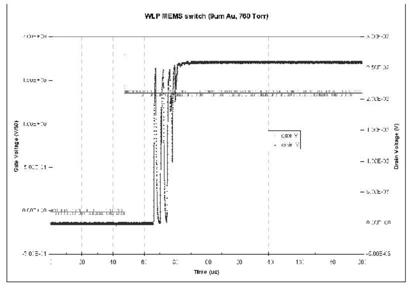
MEMS SWITCHES : **IDEAL is a controlled atmosphere conditions.**
Vacuum creates excessive bouncing -> early degradation



900 mTorr

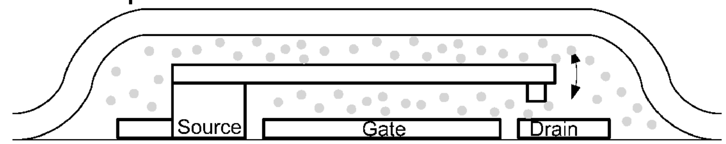


N_2 – 760 Torr

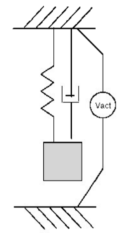


RF-MEMS Packaging Requirements

- What does pressure do for a MEMS switch?



1-D Equation of Motion



$$m\frac{d^2z}{dt^2} + b\frac{dz}{dt} + kz = F$$

Damping; Spring Constant; Applied Electrostatic Force

Viscosity of air in WLP

$$b \cong \sqrt{2}\mu_{air} L\left(\frac{W}{g}\right)^3$$

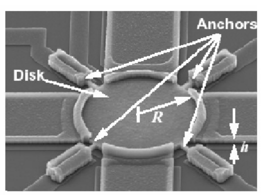
vacuum: $\mu \sim 0$ — *INERTIA-Dominated*

atm: $\mu \sim 1E\text{-}5$ kg/m3 — *DAMPING-Dominated*

- *VACCUM enhances the Q of the resonating mechanical structure*

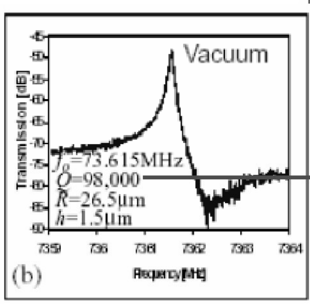
RF-MEMS Packaging Requirements

MEMS RESONATORS : **IDEAL is VACUUM – Opposite to switches!**
Atm conditions create degradation of Q factor

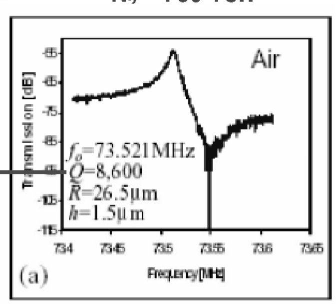


Wine-glass Resonator
(Bhave – Cornell University)

900 mTorr



N_2 – 760 Torr



RF-MEMS Packaging Requirements

- Ideal WLP environment depends on what MEMS device it is supposed to protect

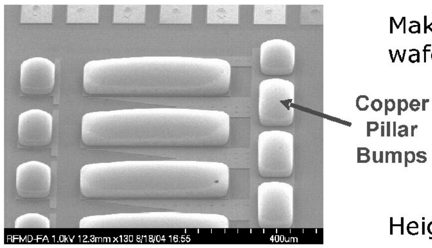
CONTACT SWITCH	~760 Torr , inert gas (must prevent corrosion of contact region) no free ions (to prevent actuator voltage spiking) no impurities left in cavity -> lifetime of contact
CAPACITIVE SWITCH	~760 Torr no free ions (to prevent actuator voltage spiking) generally less susceptible to damage than contact
RESONATORS	~100-900mTorr , Gethering metals in WLP to maintain vacuum over lifetime of part Strict hermeticity requirements or resonant frequencies may drift with time

MEMS WLP WORKSHOP

IMOC 2007

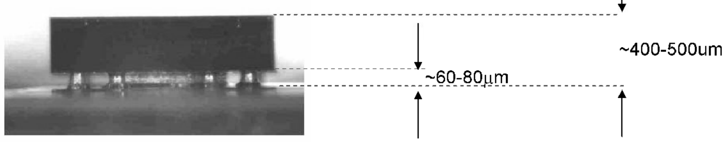
RF-MEMS Packaging Requirements

- Flip Chip Bumping : RF systems trending towards much more complex and integrated systems, requiring bumping of the different system die, including RF MEMS devices!
- WLP approach in this case must be no taller than 25-50mm!



Makes it difficult to achieve with wafer-bonding approaches

Height requirement for overall modules restricted to ~0.8mm



***** If your technology won't work here, then it won't be used in cellular applications!**

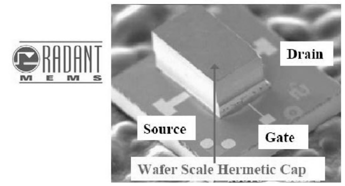
MEMS WLP WORKSHOP

IMOC 2007

Wafer-Level-Packaging Approaches

- Two distinct approaches:

Wafer-Bonding / Transfer



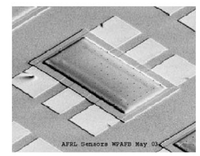
PRO's

- Easier to implement
- Easy to add desired atmosphere
- Mid-to-low cost

CON's

- Tall height requirement
- Requires wafer-to-wafer alignment / bonding
- Difficult to implement with bumping strategy

Thin-Film Encapsulation



PRO's

- Low processing cost
- Ideal for vacuum environment
- Lowest height requirement
- Ideal for applications requiring millions of switches

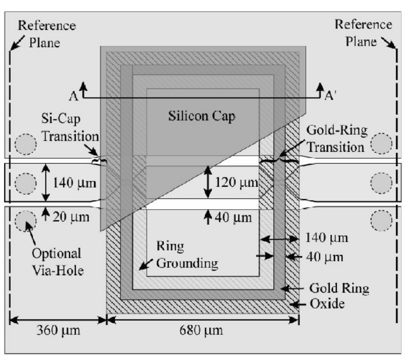
CON's

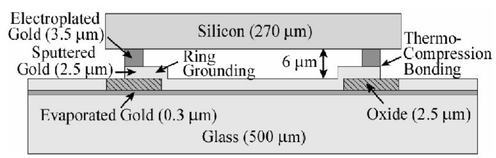
- Most difficult to engineer
- Sacrificial material critical
- Lid not very strong, must control entire assembly operation or it will fail
- Hard to seal with atm.

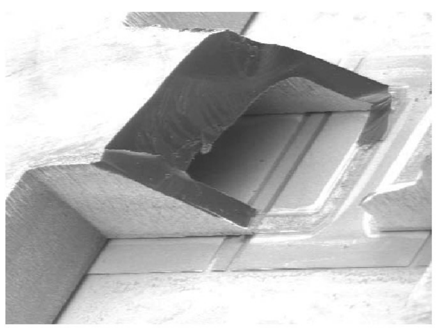
MEMS WLP WORKSHOP

IMOC 2007

WLP Processes : U of Michigan







- CPW line on glass wafer.
- Silicon cap wafer (1000 Ω-cm).
- Oxide interlayer.
- Gold-to-gold thermo-compresssion
- Bonding (360ºC, 200 N, 30 min)

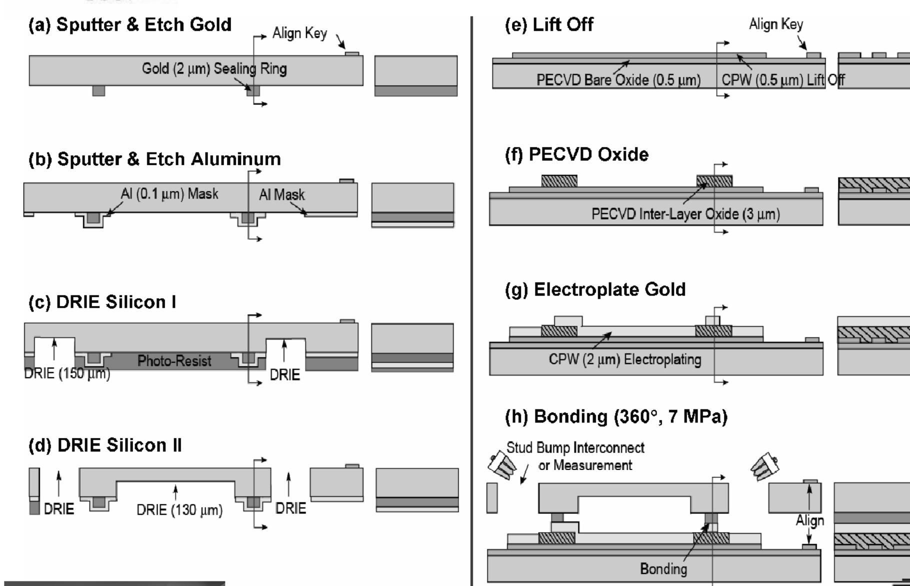
MichiganEngineering 1854-2004

UCSD

MEMS WLP WORKSHOP

IMOC 2007

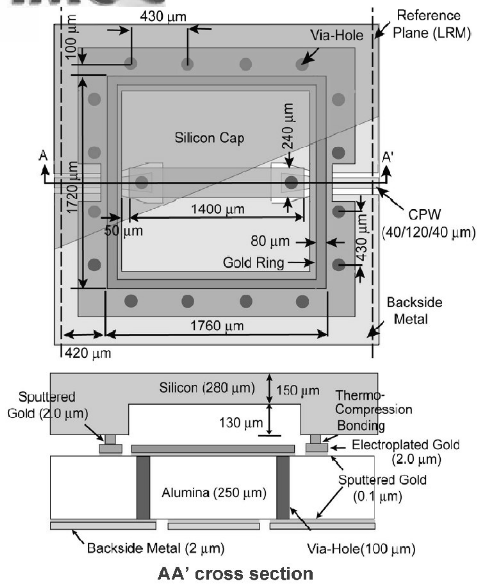
Fabrication Process : U of Michigan



MichiganEngineering 1854-2004

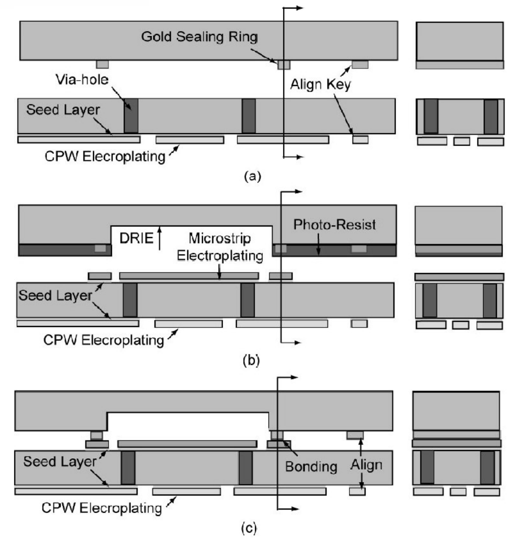
UCSD

Microstrip Packaging Design : U of Michigan



- 240 µm-wide straight microstrip line
- Silicon-on-Alumina package
- 130 µm cavity
- Gold-to-gold bonding
- Gold ring interlayer
- Via-hole transition
- Gold-ring grounding using via-holes
  - No resonance
  - Isolation

Fabrication Process



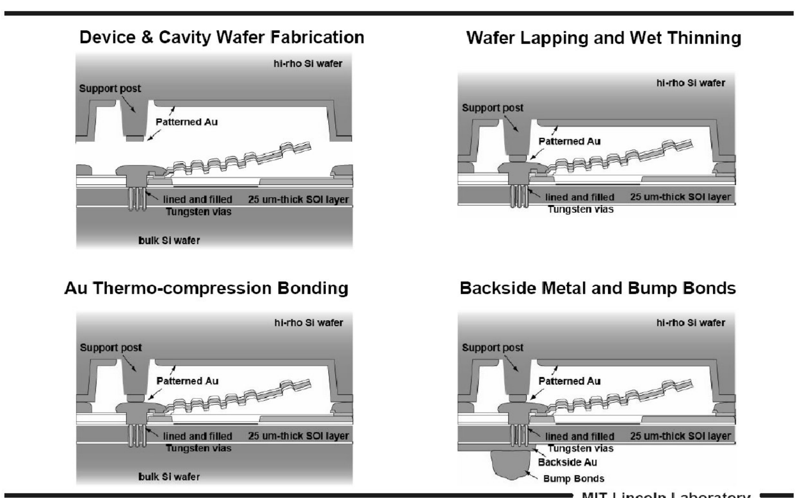
- Via-hole fabrication on bare Alumina
- Sputter, etch and electroplate gold on the backside of Alumina
- Sputter and etch gold on top of the Silicon

- Sputter, etch and electroplate gold on top of the Alumina
- DRIE etch on top of the Silicon

- Gold-to-gold thermo-compression bonding of Silicon and Alumina (320°, 7 MPa)

Lincoln Labs / MIT

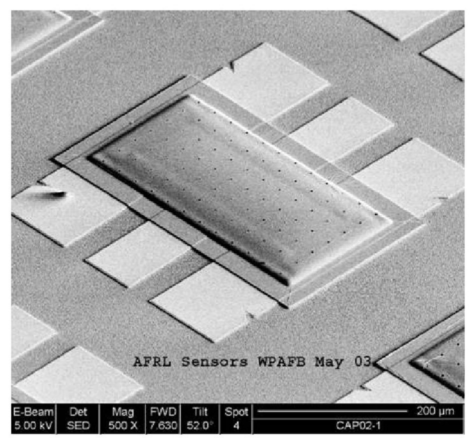
Fabrication Overview



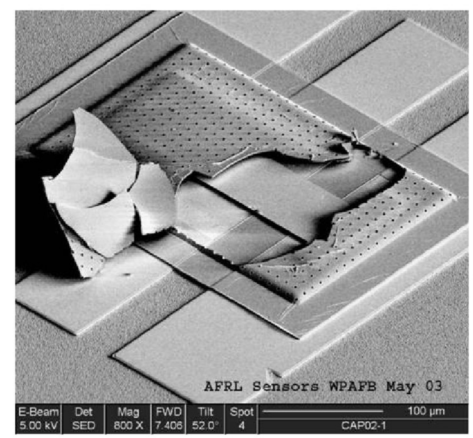
GOMAC05-10
JBM 4/6/2005

ITAR (2005)

US AIR FORCE (Jack Ebel)



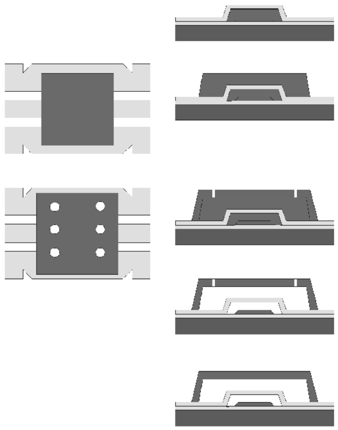
Released switch under nitride cap



Nitride cap partially removed showing released switch

US AIR FORCE Nitride Cap

Mask Layout **Side View** **Process Step**



Unreleased switch wafer

Deposit 2nd sacrificial layer
PMGI, 3.0 μm

Deposit dielectric capping layer
Sputtered Si_3N_4, 1.7 μm

Release switches through access holes
Wet release, Supercritical CO_2 dry

Seal access holes
PECVD SiO_2, 2.0 μm, 300°C

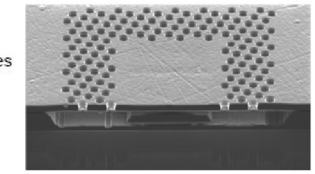
ITAR (2005)

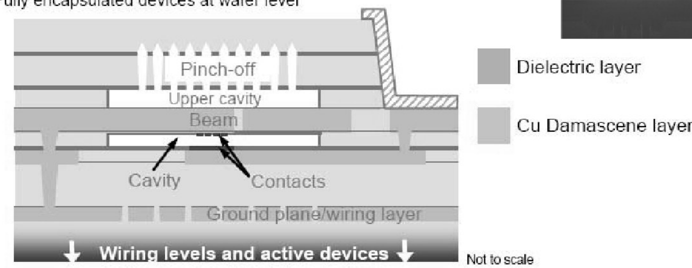
IBM MEMS WLP

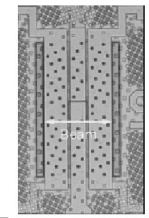
IBM T.J. Watson Research Center

Integration Approach

- MEMS switches and resonators which can be integrated within the wiring levels for SiGe or analog CMOS IC's
  - Better performance, smaller size than separate components
  - Potential for lower assembled cost as technology matures
  - Could enable novel radio architectures requiring many MEMS devices
- Devices built in a CMOS manufacturing environment with no new tools
- Process flow that allows fabrication of multiple types of devices
- Fully encapsulated devices at wafer level







6 | June 2005 | IBM RF-MEMS, IMS 2005 Friday Workshop © 2004 IBM Corporation

SUMMARY

- Unless you can afford expensive ceramic packages, packaging is an integral part of engineering the MEMS device.
- Bonded-wafer capping approaches (w/ metal/dielectric/solder etc) bonding methods are in wide use in MEMS switches. Issue: larger size, tall height requirements, mid-level cost. But if it works for you, this is the most straight forward path.
- Thin-film encapsulation suits capacitive switches better than contact switches. By far the cheapest method, and also the only one which yields truly miniaturized MEMS devices. But also the hardest approach of all methods. Tricky to seal under anything but vacuum.
- This is a fluid R&D area. RF MEMS are actually just now coming into the market. There is time for your great novel packaging idea to be a success….But don't wait too long!

Multi-Physic issues for RF MEMS Simulation and Design

Robert PLANA

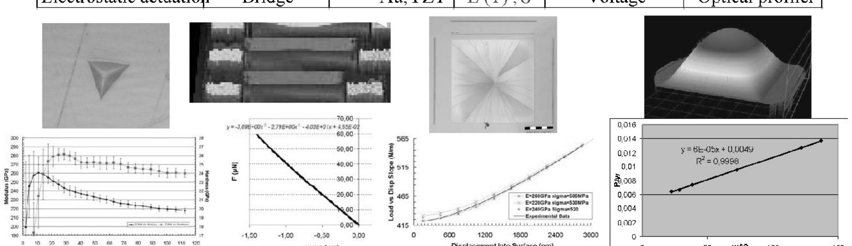
- Agenda
  - Introduction
  - MEMS process simulation
  - Developement of new test set for material and process characterization
  - Contact simulation
  - EM-Thermal simulation
  - Conclusive remarks

Introduction

- RF MEMS has demonstrated attractive performance
- Technology based on Electromechanical and electrothermal coupling
- Need to have materials properties (thin films essentially)
- Need to perform Multi-physic simulation
- Simulation as a tool for process and device optimization

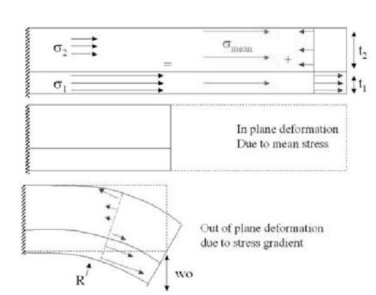
MECHANICAL and dielectric PROPERTIES OF MATERIAL

Measurement technique	Test structure	Material	Properties	Loading	Deformation
Wafer curvature	Full wafer	All*	σ	*****	Profiler
Cantilever curvature	Cantilever	Au	Δσ , σ**	*****	Optical profiler
Nano indentation	Full wafer	SiNx , Au , Cu	E , σ	Nano indentor	Nano indentor
Ponctual loading	Bridge	Au	E , σ	Nano indentor	Nano indentor
Ponctual loading	Membrane	SiNx , Au	E , σ , σ_r	Nano indentor	Nano indentor
Bulge test	Membrane	SiNx , Au	E , σ , σ_r	Pressure	Optical profiler
Vibrometry	Bridge	Au,PZT	E , σ	Piezoelectric	Optical profiler
Vibrometry	Membrane	Au, PZT	E , σ	Piezoelectric	Optical profiler
Electrostatic actuation	Cantilever	Au σ	E (T) , σ	Voltage	Optical profiler
Electrostatic actuation	Bridge	Au, PZT	E (T) , σ	Voltage	Optical profiler

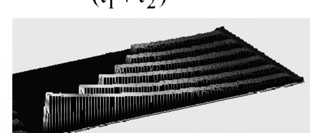


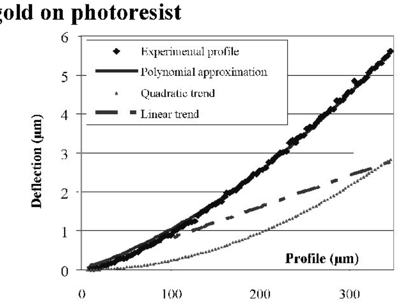
STRESS CONTROL IN EVAPORATED GOLD

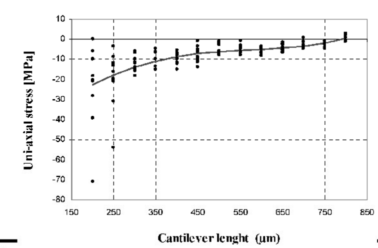
Stress measurement in evaporated gold on photoresist



$$w = \frac{3\ t_1 t_2}{(t_1 + t_2)^3} \frac{\sigma_{u1} - \sigma_{u2}}{E} L^2$$







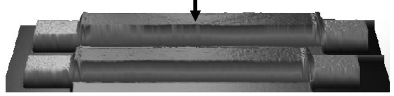
Karim Yacine

PONCTUAL LOADING OF GOLD BRIDGES

☞ **Analytical model : Cte evaluation with numerical parametric model**

$$K = K_L + K_\sigma = cte_1 \cdot \frac{E}{1-\nu^2} \cdot \left(\frac{t}{L}\right)^3 \cdot b + cte_2 \cdot \sigma(1-\nu)\left(\frac{t}{L}\right) \cdot b$$

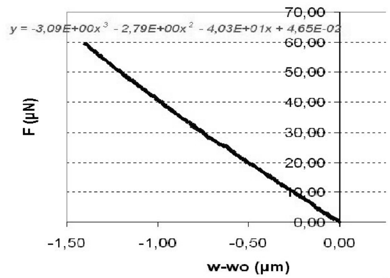
cte1 = 13,4 +/- 4% (Perfect anchorage : cte1 = 16)
cte2 = 4,11+/- 5% (Perfect anchorage : cte2 = 4)



☞ **Stiffness measurement of different bridge lenght**

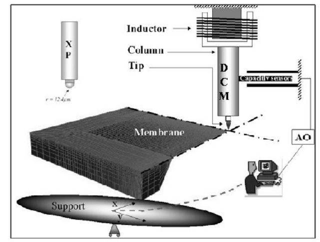
K . L (1/L²) → slope ∝ E

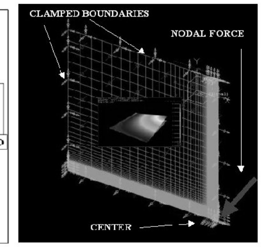
K . L³ (L²) → slope ∝ σ

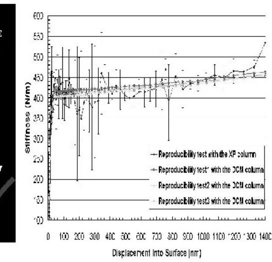


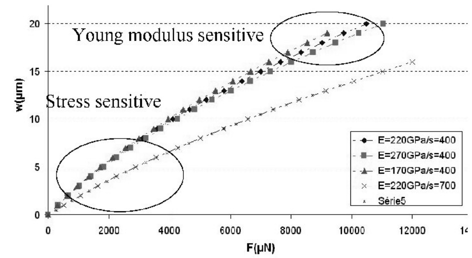
PONCTUAL LOADING of SiNx MEMBRANE

☞ **Ponctual loading on membrane center** → Local deformation





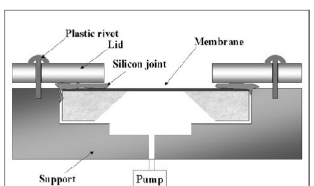


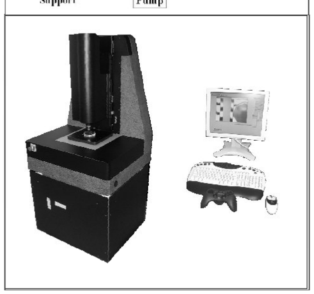


☞ **Membrane fracture before enough high deflexion :**
- σ and σ_r evaluation
- E : impossible

→ Fabrication of dielectric bump on membrane center

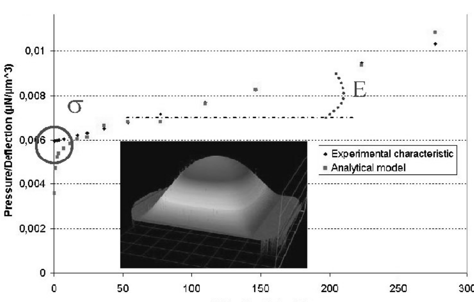
BULDGE TEST of SiNx MEMBRANE





$$P = C_1 \frac{t.\sigma}{a^2}.w + C_2(\nu).\frac{t.E}{a^4.(1-\nu)}.w$$

Numerically or analytically determined

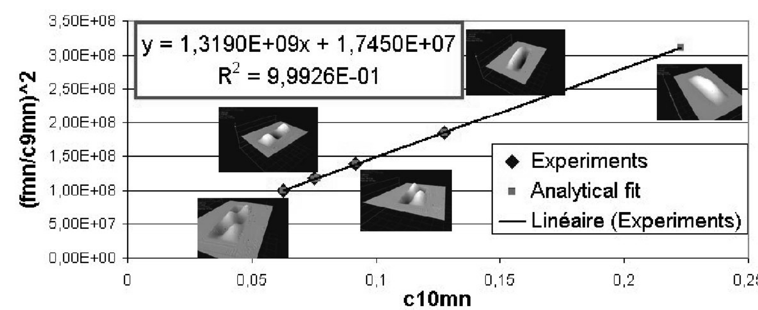


VIBROMETRY (Gold membrane)

Simplified analytical formulation (for squared membrane) :

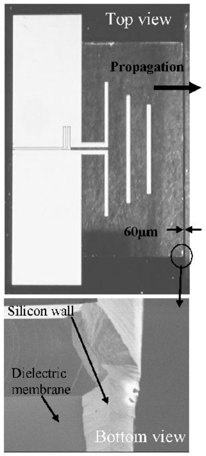
$$\left(\frac{f_{mn}}{C_{9mn}}\right)^2 = \frac{\sigma}{\rho a^2} C_{10mn} + \frac{E}{\rho(1-\nu^2)}\left(\frac{h}{a^2}\right)^2$$

Analytical constant

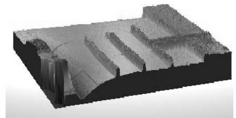


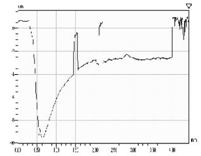
OPTIMISATION OF QUASI FREE-EDGE MEMBRANE

Yagi Antenna

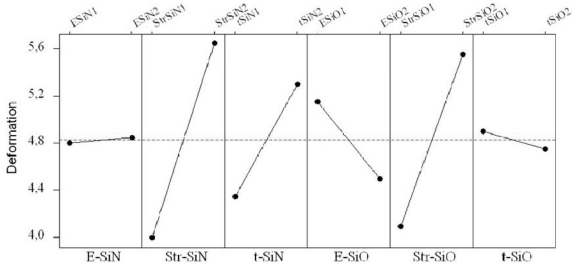


SiO2 /SiNx membrane





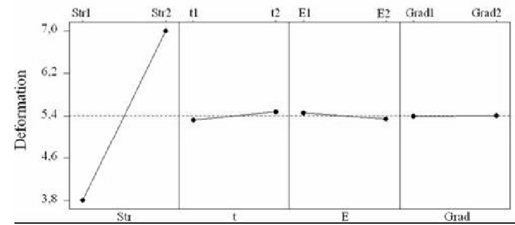
DOE and FEA simulation of quasi free edge membrane



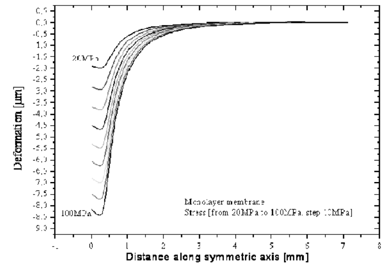
- Main effect of stresses in layers
- Difficult to optimize related to stress control

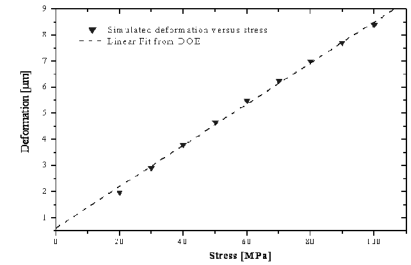
OPTIMISATION OF QUASI FREE-EDGE MEMBRANE

DOE and FEA simulation of quasi free edge membrane (SiOxNy membrane)



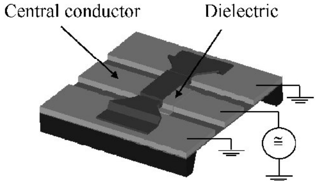
- $\sigma \cong$ 20MPa ± 20MPa
- 0.6µm < Deflection < 3.8µm

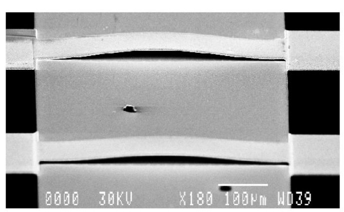




Thermomechanical simulation of RF MEMS process

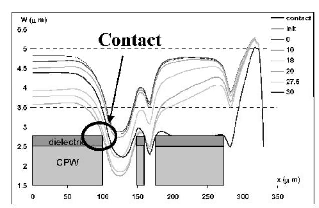
Mechanical operation of MEMS are highly dependant upon **stresses** and **geometry** and their couplings **at end of process**

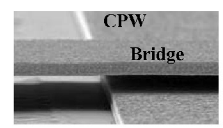




HIGH ISOLATION of CAPACITIVE SWITCH

- **Good contact between dielectric on CPW lines and Bridge**
  - ⇨ Bridge shape





Packaging process simulation

Bonding process simulations

The seal is compressed between a stationary plane surface defined by the cap and a structured surface made of the gold conductor (Fig. 9)

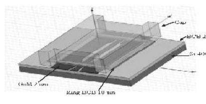


Figure 8 : 3D Model

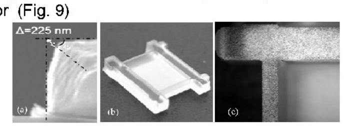


Figure 9 : (a) Gold conductor profile - Micro-machined Foturan cap– Bottom sight (b) and (c) Zoom on the RF wall of 200 um

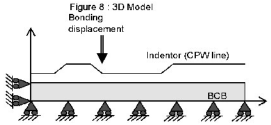


Figure 10 Model definition (half structure due to symmetry)

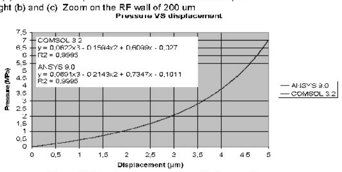


Figure 12 Bonding pressure versus displacement

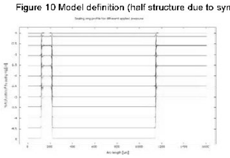


Figure 11 BCB displacement vs pressure bonding

A minimal pressure of 1.5 MPa is need to allow the contact between the BCB and CPW gap

FEMLAB and ANSYS Software's were accurate within 0.3% each other

Materials characterization for very low voltage actuator

Material characteristics	value	method	instrument
Strain coefficients	d31	Full sheet	AFM
		Full sheet	d33 meter
		cantilever	Fogale
	d33	Full sheet	AFM
		Full sheet	d33 meter
		cantilever	Fogale
Dielectric constant		Full sheet	MIM capacitor
Electrical conductivity		Full sheet	
Residual Stress		Full sheet	Fogale
Hardness		Full sheet	Nano-Indenter
		Bridge	Nano-Indenter
Young modulus	E	Full sheet	Nano-Indenter
		Bridge	Nano-Indenter

Basic design rules for the capacitor plate

- Dielectric materials {AlN; PZT}
- Capacitance tunable range : 0.5…20 pF
- Determination of the gap (capacitance ratio)
- Determination of the area (maximum capacitance value)

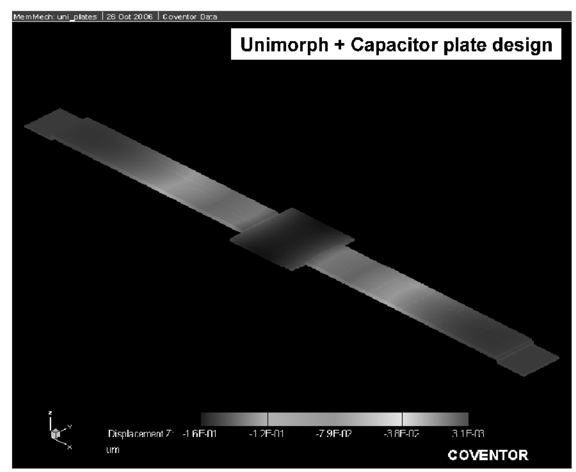
$$d_{gap} = (\tau - 1)\frac{d_k}{\varepsilon_k}$$

$$A = \frac{d_k C_{max}}{\varepsilon_0 \varepsilon_k}$$

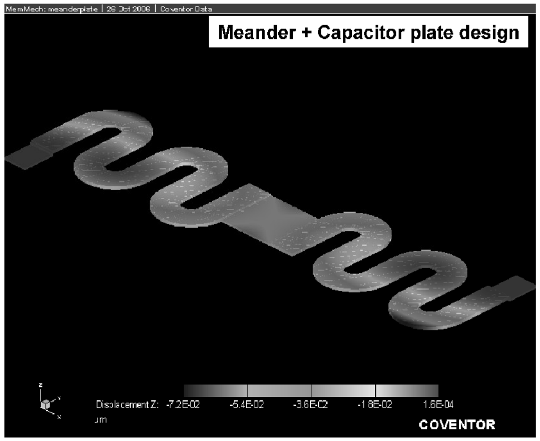
$$\tau = \frac{C_{max}}{C_{min}}$$

	AlN	PZT
Thickness [µm]	0.2	0.2
Permittivity	10	100
Gap size [µm]	0.8	0.08
Area [µm x µm]	215x215	70x70

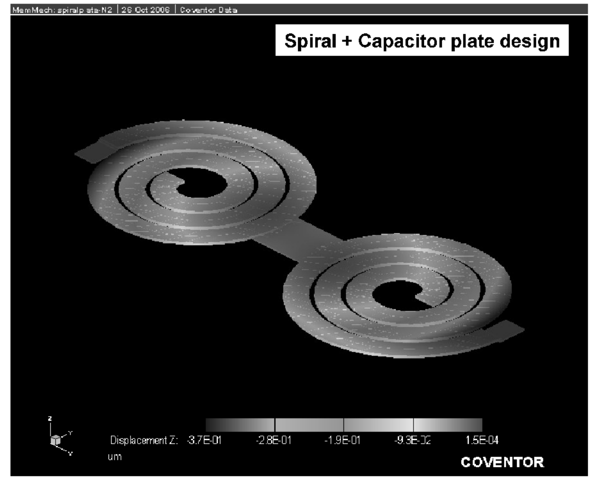
Actuator & Capacitor Overview



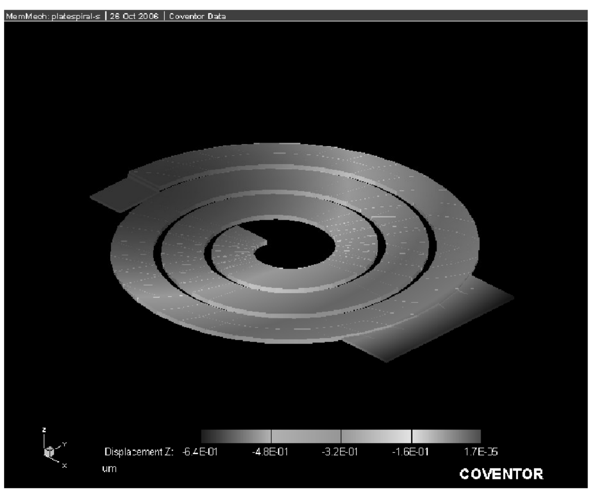
Actuator & Capacitor Overview…2



Actuator & Capacitor Overview…3

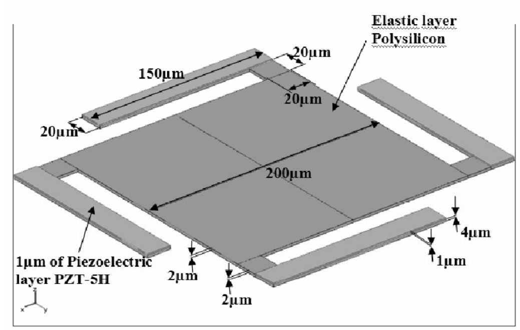


Actuator & Capacitor Overview…4



Very low voltage actuator

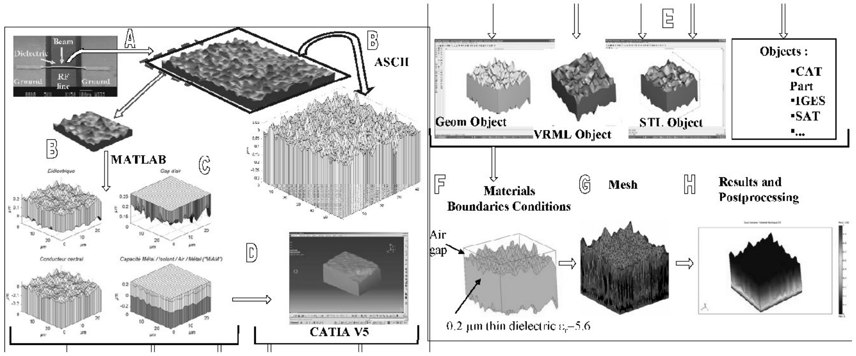
This capacitor plate structure was simulated on both softwares and the results were within 1% of error which is acceptable but COMSOL showed rapidity 10 times more than ANSYS.



Software	COMSOL	ANSYS	ANSYS
Mesh size (µm)	10	5	1.25
Max Von Mises stress (MPa)	129	73	123
Max deflection (µm)	0.8165	0.793	0.821
Calculation time (seconds)	22	33	690

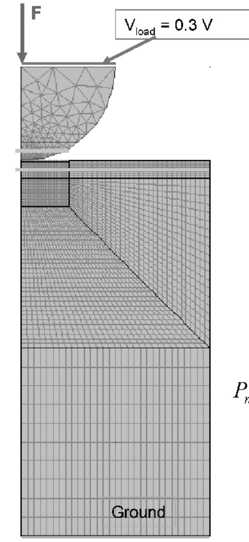
Capacitive contact calculation by reverse engineering method

- **Good contact between dielectric on CPW lines and Bridge**
  - ⇨ Roughness and picks height of gold CPW
  - ⇨ Roughness and picks of under bridge side

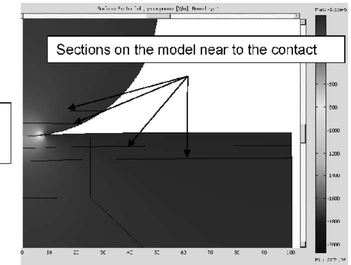


Perfect contact : 3pF
Measurement : 1.4pF
Simulated : 1pF

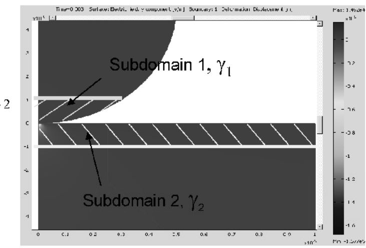
METAL/METAL CONTACT MODELLING



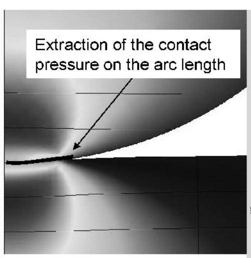
$$R_{tot} = R_{cylinder} + R_{contact} + R_{block}$$

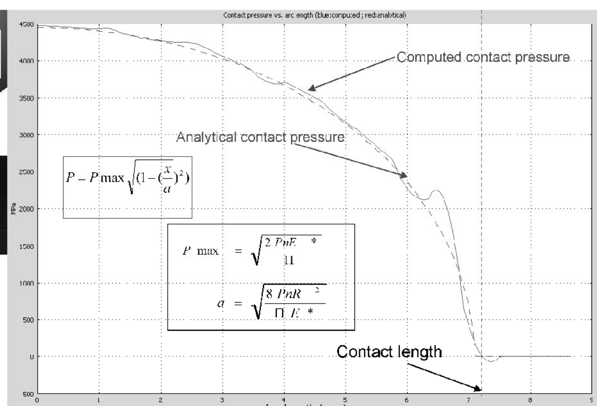


$$P_n élec = \iint \frac{j^2}{\gamma_n} L dS = R_n i^2$$



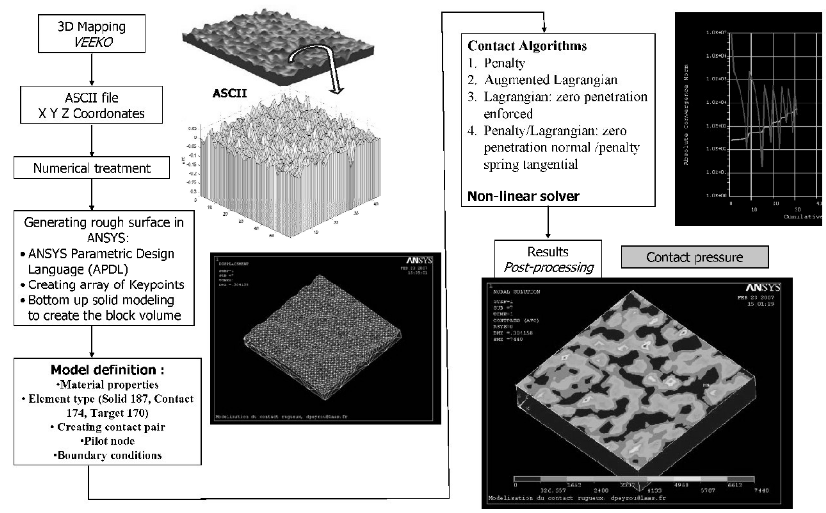
METAL/METAL CONTACT MODELLING





Contact pressure along the contact area for both the analytical and the COMSOL Multiphysics solution

METAL/METAL CONTACT MODELLING with Reverse engineering method



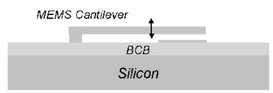
Problem: RF Induced Heat

- ✓ *Increasing working frequency (mm and µm-wave range)* $f\uparrow$
- ✓ *Needs of high RF power levels (beyond 5W)* $P_{RF}\uparrow$
- ✓ *Downscaling into µ- and n-meter range (IC technology)* $l\downarrow$

$$\Rightarrow \quad Q \propto \frac{1}{(l\downarrow)^2}\left(f\uparrow P_{RF}\uparrow\right)^{\frac{1}{2}} \Rightarrow \left(Q\uparrow\right)^3$$

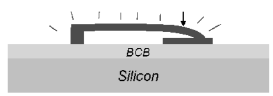
Heat (power losses by Joule effect) ***<u>may increases by power 3</u>***

- *Use of material (BCB) with poor thermal properties impedes dissipation*
  ⇒ ***High temperature rise*** $\Delta T\uparrow$



⇩

- *Mechanical compliant structures (MEMS)*
  ⇒ ***Mechanical deformations***



Motivations

Power handling RF MEMS systems

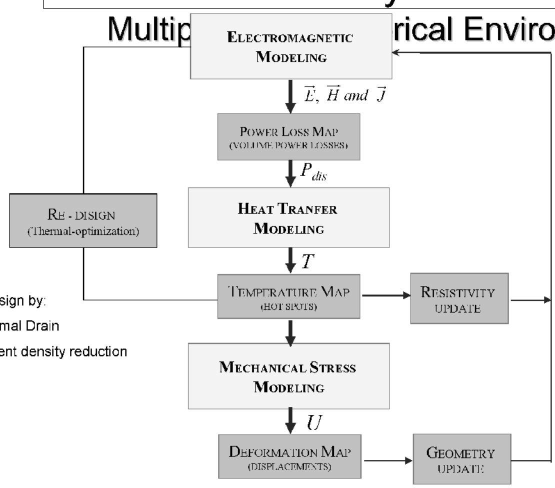
NEED

*<u>Concurrent</u> Electromagnetic – Thermal – Mechanical Design (**<u>Co-design</u>**)*

Define a multiphysics numerical environment for the *Electromagnetic – Thermal – Mechanical* modeling is strongly demanded in order to carry out **analysis and optimization** (before the fabrication with enormous time and costs saving)

Electro-Thermo-Mechanical Analysis

Multip rical Environment



Re-dsign by:

- Thermal Drain
- Current density reduction

Modeling Flow

FREQUENCY DOMAIN — ELECTROMAGNETIC MODELING

Result of the full-wave analysis: $\vec{E}, \vec{H}, \vec{J}$

$$P_{dis} = \frac{1}{2}\Re\left\{\int_V \vec{E}\cdot\vec{J}\,dV\right\} + \frac{\omega}{2}\left\{\int_V \varepsilon''\left|\vec{E}\right|^2 dV + \int_V \mu''\left|\vec{H}\right|^2 dV\right\}$$

Losses in conductors — *Losses in dielectrics and magnetic materials*

TIME DOMAIN — HEAT TRANFER MODELING

$$\rho c_p \frac{\partial T}{\partial t} = k\nabla^2 T + P_{dis}$$

Conductive heat transfer (Fourier Law)

T temperature; ρc_p *thermal inertia; k thermal conductivity.*

Convective and Radiation heat transfer are considered but give a minor contribution

TIME DOMAIN — MECHANICAL STRESS MODELING

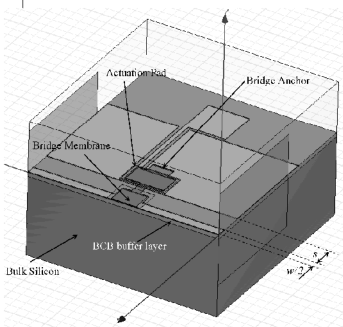
$$\bar{\bar{\sigma}} = \bar{\lambda}\, trace(\bar{\bar{\varepsilon}})I + 2\bar{\mu}\bar{\bar{\varepsilon}} - \frac{E}{1-2\nu}\alpha(T-T_0)I$$

Constitutive equation for the Stress tensor (isotropic elastic material)

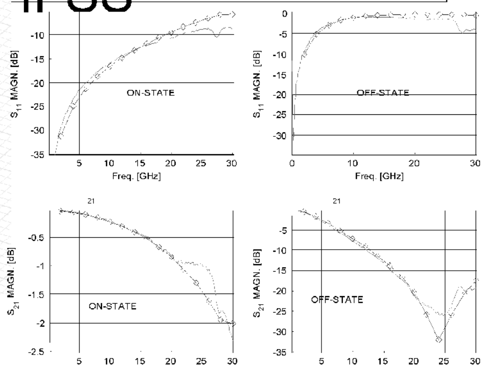
$$\bar{\bar{\varepsilon}} = \nabla^{(S)} u$$

<u>Linear relation</u> between strain tensor and deformations

Electromagnetic Model by HFSS



Half Structure Model View



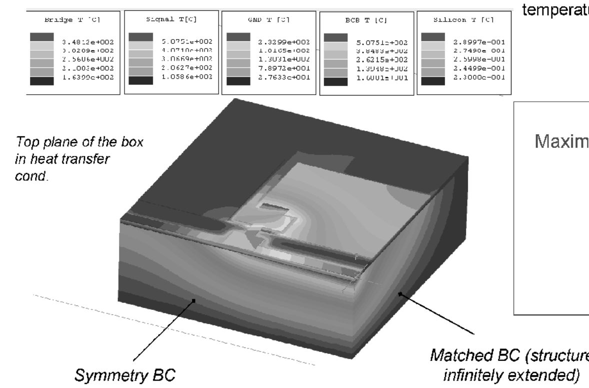
Shunt Capacitive MEMS Switch: Gold CPW line on BCB/Si substrate (20/400µm)

HFSS. (BLUE); Measured (MAG)

Thermal Modeling by e-physics:

Thermal transient over 0.5sec: OFF-STATE @ 24GHz and 6 W Input Power

Temperature Distribution at steady-state (after 0.5 sec.): Device originally at room temperature of T0=23°C



Maximum Temperature on the signal line:
Tmax=507°C

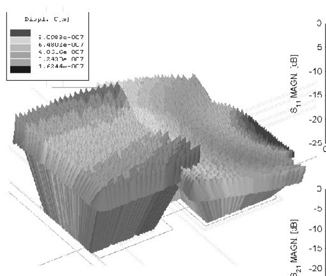
On the bridge
Tmax=348°C

The scales are different for better representation

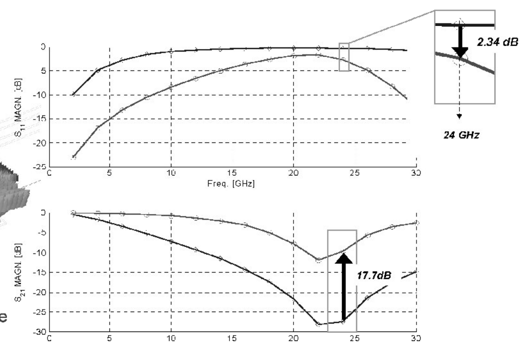
Mechanical Deformation Modeling by e-physics

OFF-STATE @ **24GHz** and 6 W Input Power

The displacement computed with e-physiscs are mapped back to HFSS for a re-simulation



Deformation Distribution on the Bridge



Original (-○—○-) Deformed (-o—o-)

General Consideration and Co-design

High RF power level (above 5W) in RF-MEMS device based on excellent structuring and electrical material, but with very low thermal conductivity (as BCB) may yields hot spot at temperature above the technological tolerable limits and serious (thermo mechanical) side effects.

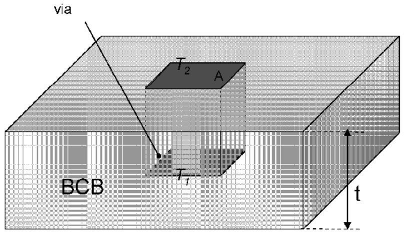
TWO possible solutions (re-designs) are here considered:

- ✓ Thermal drain (via)
- ✓ Current density reduction (smoothing the distribution)

In both cases the electromagnetic and mechanical performances *are effected*, therefore concurrent design (co-design) approach is needed.

Re-design: Improving Thermal Drain

Thermal Via through BCB



$$\Delta T = T_2 - T_1 = Q\frac{R}{A}$$

Where
Q is the heat flow through the layer
T_2 is the top object temperature
T_1 is the bulk silicon temperature (considered constant)
A area of the via
R is the thermal square resistance given by

$$R = \frac{t}{k} \quad [m^2K/W]$$

K is the thermal conductivity ***(k_{BCB}=0.29 W/mK)***

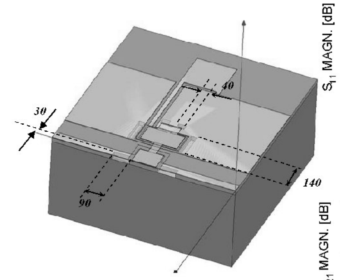
Example: In order to keep the ΔT_{max} = 150°C for a given RF power losses of P_{dis}=Q=100mW and for t=20µm the via area should be:

$$A = P_{dis}\frac{t}{\Delta T\ k} = \begin{cases} 90\ \mu m^2 \text{ for } \mathbf{k_{Si}=148W/mK} \\ 42.3\mu m^2 \text{ for } \mathbf{k_{Au}=315W/mK} \end{cases}$$

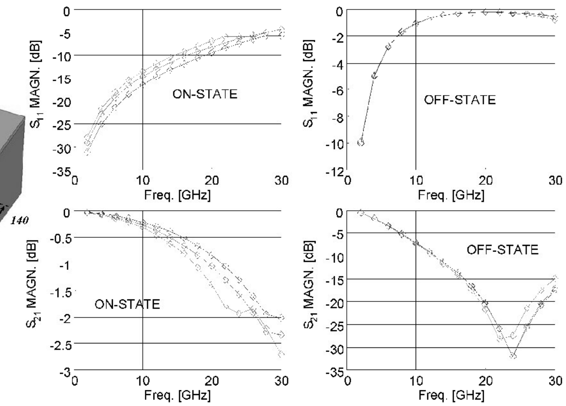
***Si-via* must have 2.13 times the cross-section area than gold ones in order to drain the same amount of heat.**

Re-design: ImprovingThermal Drain
Effect of thermal drain on the electromagnetic performances.

Use of Au via is preferred to Silicon ones (due to high losses 2000Ω cm⁻¹)



Introduction of Via through the BCB buffer layer. Area A_{Au}=16.2 $10^{-9}m^2$)



Orig. (BLUE); Au-via (RED); Si-via (MAG)

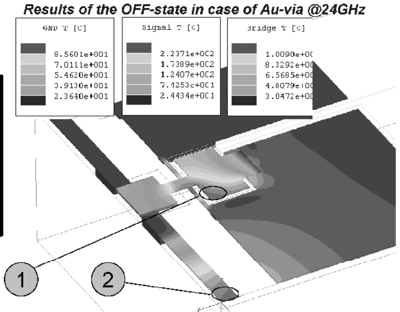
Re-design: Thermal Modeling Results

Comparison for ON/OFF state in case of Si-via at 2 freq.

Design		T_{max} (Global) [°C] 10 GHz	T_{max} (Global) [°C] 24 GHz	T_{max} (on bridge) [°C] 10 GHz	T_{max} (on bridge) [°C] 24 GHz	Umax [µm] 10 GHz	Umax [µm] 24 GHz
O	ON-State	72.5	163	55	101	0.05	0.15
	OFF-State	162	507	106	348	0.2	0.81
R	ON-State	59.9	144	35.3	50	0.04	0.01
	OFF-State	107	180 (3)	37.3	64 (4)	0.02	0.06

O = Original design
R = Re-design with Si Via

Results of the OFF-state in case of Au-via @24GHz



In case OFF-State @ 24GHz and 6W

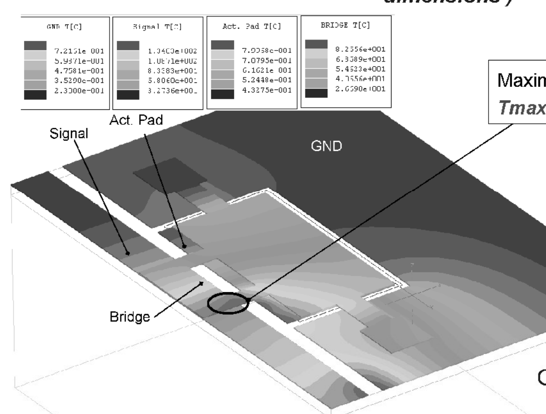
Original design:
T_{max}(global)=507°C
T_{max}(bridge)=348°C

T_{max}(global) = 223°C (1)
T_{max}(bridge) = 101°C (2)
Au Thermal via

T_{max}(global) = 180°C (3)
T_{max}(bridge) = 64°C (4)
Si Thermal via

Re-design: Current Density Distribution

Layout Re-designed in order to reduce the Current density and therefore the induced heat (enlargement of CPW dimensions)

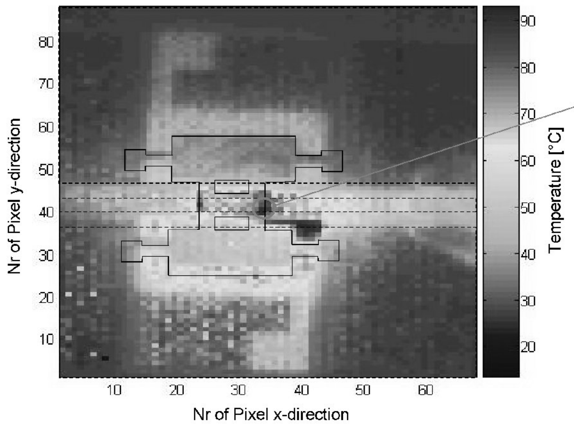


Maximum Temp on the bridge
Tmax=82.6°C *(e-physic MODEL)*

OFF-State @ **10GHz** and 6 W

Experimental Validation by IR Camera

Temperature mapping at (Steady-state) 10GHz and 6 W



MEASURE

Maximum Temp. (on the bridge):
Tmax= 88±5°C

e-physic MODEL

Maximum Temp on the bridge:
Tmax=82.6°C

Agreement within 10%

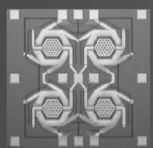
The pixel size is 20x20µm^2 and the membrane shape contour is marked in black

Conclusive remarks

- **Material characterization is essential for MEMS process understanding**
- **Process simulation can help to optimize process flow for future industrialization**
- **Multi-physic simulations efficient tool for contact simulation**
- **Contact simulations as a tool for Physic of Failure simulation**
- **A complete electro-thermo-mechanical modeling chain (based on commercial software - Ansoft Corp.) has been presented and tested on RF MEMS switches**
- **Low thermal conductivity structuring materials (BCB) <u>impedes the heat drain</u> and yields hot spot temperatures above 500°C (CPW signal line) and above 300°C on suspended parts (bridge) for working RF power above 5W (@ 24GHz).**
- **Two possible approaches have been proposed in order to avoid critical temperature rises:**
  - **Increasing of thermal drain by introducing thermal via through the BCB**
  - **Decreasing of the current density distribution**
- **These approaches have been successful validated. The hot spot temperature has been reduced down to 64°C for the Si via and 101°C for the gold one (for 6W @24GHz).**
- **Thermal numerical results have been validated by IR camera with agreement within 10%**
- **The presented modeling environment plays a crucial role in analysis and optimization of integrated MEMS devices into power handling RF front-end**

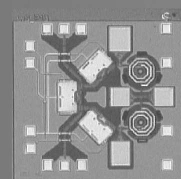
Multi-band and Multi-mode RF MEMS

Architectures & Front-Ends



Dr. Art Morris

wiSpry, Inc.



wiSpry Intro

- Fabless product company
  - High-performance low-cost "spry" RF components
- 28 Employees, Headquartered in Irvine California
  - Raised > $22M in Venture Capital
- Established in October 2002; Spun-Out of Coventor
  - Team developing Wispry Core Technology Since 1999
- Sampling Customers with Tunable "Filter" Products
  - Limited Shipments in late 07
  - High volume late 2008

COVENTOR® → wiSpry

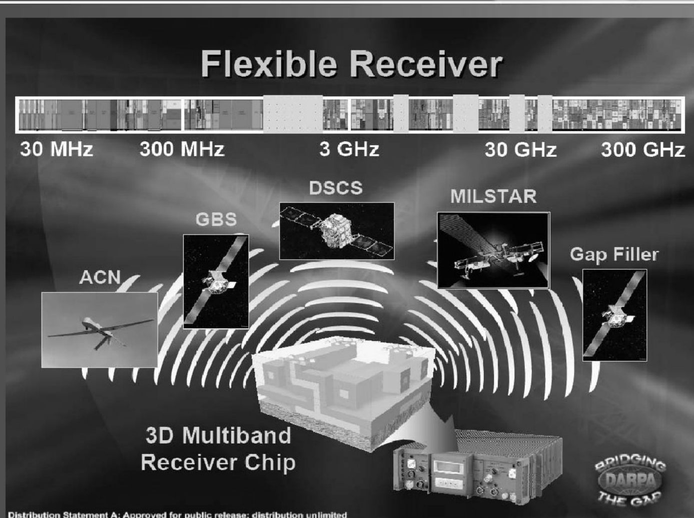
Agenda

- Motivation
- Types of RF-MEMS
- Approaches to System Solutions
- Required Sub-systems and Components
- MEMS Solutions
- Q&A

Two Related Key Opportunities

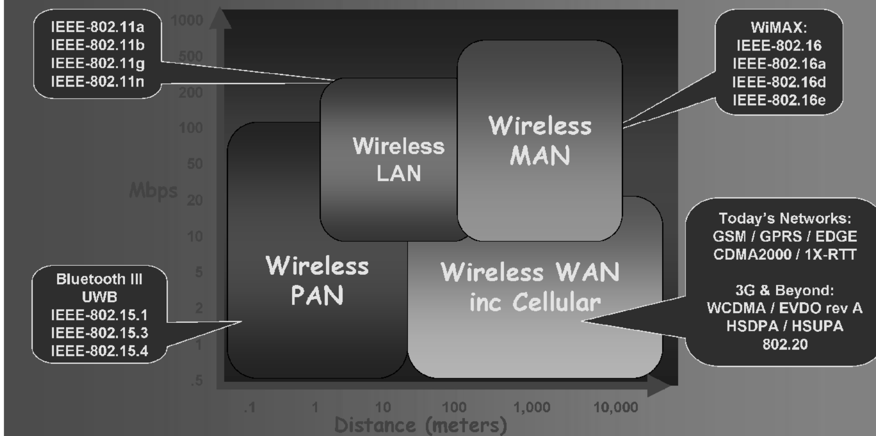
- Performance at the Bleeding Edge
  - Radar and Communication
  - Directionality and Frequency Control
  - Agile front ends for software-defined radio (SDR)
  - Adaptability
    - Utilize any available spectrum
    - Dynamically optimize performance
- Optimum Integration for the Masses
  - Multi-band handsets with smaller, lower-cost RFE
  - Multi-national products reduce inventory issues
  - Increase economies of scale through adaptability
  - Improve coverage and battery life
  - "Future-proofing"

Military/Aerospace Systems



Source: DARPA

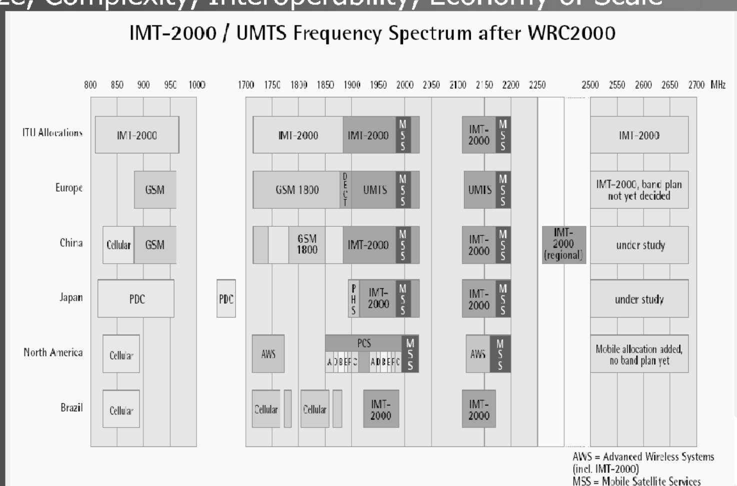
Evolving Wireless Technologies



... Yield new Wireless Bands and Standards

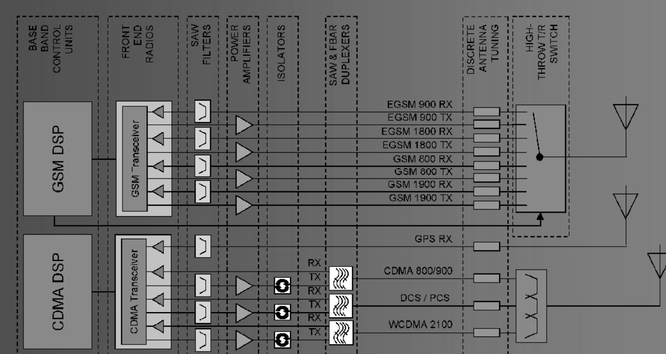
Cellular Band Proliferation

- Size, Complexity, Interoperability, Economy of Scale



Multi-band Phone Challenge

- **Multi-band / Multi-mode phones are populated by a great many active and passive components, which occupy space, impact performance, and cost $$**

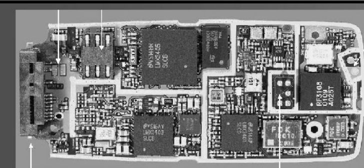


Increasing Radio Complexity

- Proliferation of new Standards and new Frequency Bands
  - Each Additional Band has its own Filter
  - Each New Standard has its own Unique Filter Requirements
- 3G Phones (CDMA & WCDMA)
  - Require Additional Costly Duplexer
  - Increased Loss, Lower Sensitivity, Lower Battery Life
- 'Diversity Receive' and MIMO Systems use Multiple Radios
  - Each with its own RF Chain
  - Each Requiring Additional Filters, Switches, etc.
- Actives and Passives Proliferate!

Challenge -> Opportunity

- Communications Designers Challenged to Provide More (Features, Bandwidth, Talk Time, Range, Interoperability, Adaptability, …) with Less (Development Time, Power, Size, Cost, …)
- Digital Integration proceeds apace but Lack of RF Integration (Capability) Limits Scaling



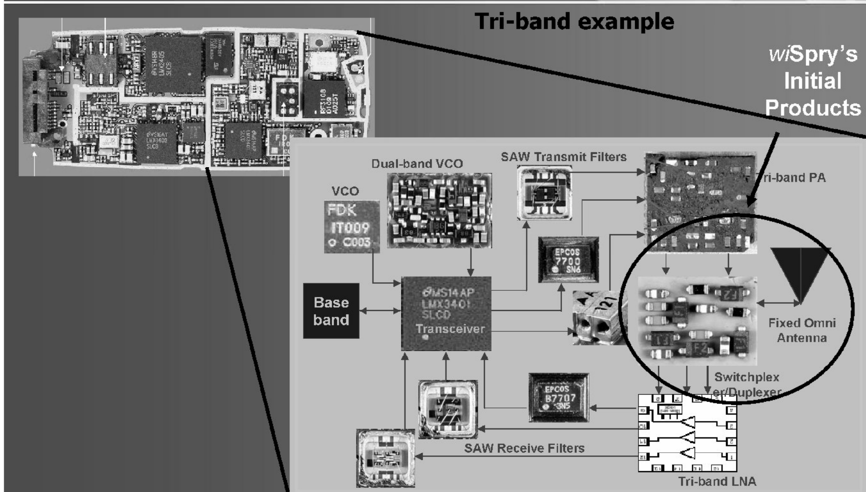
Example Cell Phone

Total Board = 30 cm^2

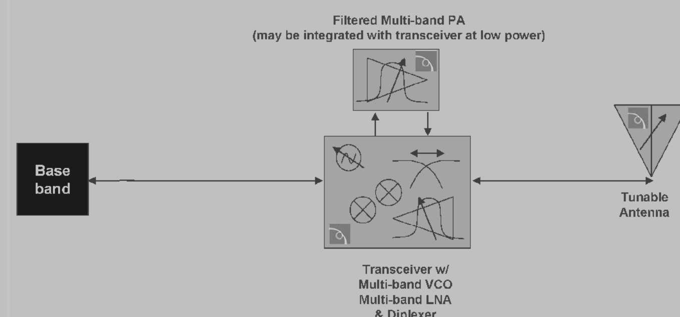
RF Section = 13 cm^2 (44% and rising)

Vision: Re-configurable RF Front-Ends

Tri-band example



Vision: Re-configurable RF Front-Ends



Benefits
- Lower Overall Cost (Savings of 50-75% Possible)
- Much Smaller Footprint
- Improved RF Performance
- Faster Time to Market

Hardware Needed to Fulfill Vision

- Highly Linear Selective Elements
- Tunable and/or Reconfigurable
  - Antenna
  - Duplexing (TDD or FDD)
  - Front-end filter
  - Power Amplifier
  - Harmonic Filter
  - LNA
  - VCO
  - Mixer
  - IF filter
  - Matching Network

Technological Options - Integration

- Discretes
  - Highest performance
  - Mostly for Mil/Aero
- SIP
  - High Performance
  - Make optimum monolithic choices for yield
  - MCM and Chip Stacking
  - Package Passives (LTCC, etc.)
- SOC
  - Lowest Cost only if functions are stacked
  - Performance Penalty
  - Yield Challenge
  - Interference Issues

Technological Options - Devices

- Semiconductors
  - Mature industry with long track record
  - Always advancing
  - Still a long way to go in performance and linearity
- Ferroelectrics
  - Linearity and stability still an open question
  - Monolithic integration with control not yet feasible
- MEMS
  - Highly linear
  - Performance superb
  - Monolithically integratable
  - Not yet proven in high volume

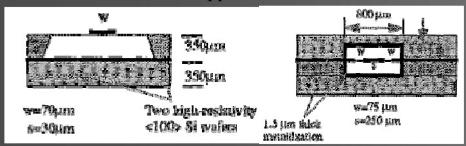
MEMS – Micro-machining

Transmission Lines

Maintain 50Ω at small dimensions

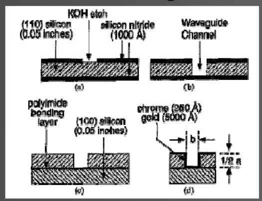
With losses < 1dB/cm at 10 GHz

Membrane Supported Lines



U Michigan

Micromachined Waveguides

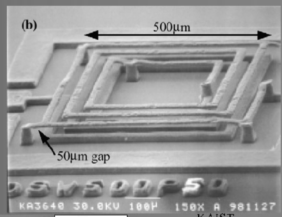


JPL, CIT, IEEE

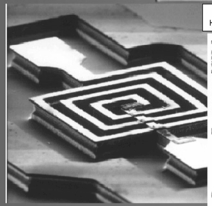
Inductors

L > 14 nH

Q up to 100 at 2 GHz



KAIST



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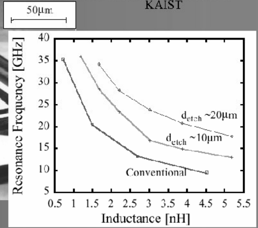
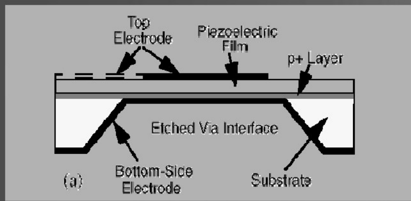


MEMS - Resonators & Filters

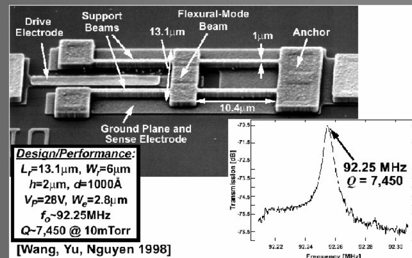
Thin-film Bulk



RF up to 7.5 GHz
Q > 1000

Agilent and Infineon shipping FBAR/BAW-based SAW-replacement filters.

Flexural Mode



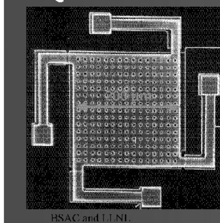
IF above 90 MHz & Q > 7000
RF above 1GHz & Q > 10000

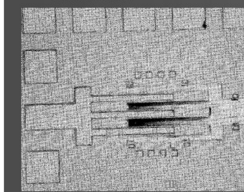
Discera shipping oscillators stabilized with IF resonators.
SiTime shipping resonators.

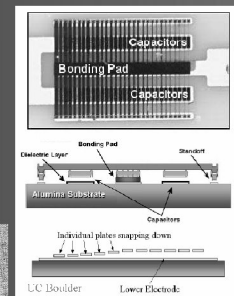
MEMS - Varactors and Switches

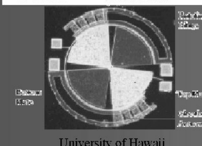
Capacitance > 8 pF
Ratios > 10:1
Q > 200 at 2 GHz

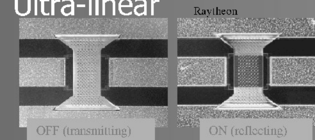
Low Loss < 0.1dB
High Isolation > 50 dB
Ultra-linear

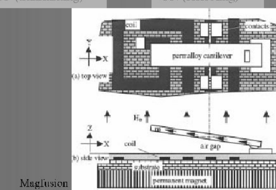


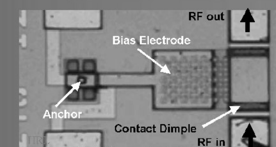










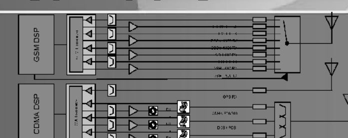


Key Challenges for RF-MEMS

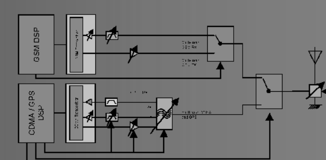
- Why are RF-MEMS not already in widespread use?
  - MEMS dominate accelerometer and projection display markets
- Cost
  - Hermetic sealing and packaging
  - Size and complexity of overall solution – added passives
  - Integration barriers – individual device is rarely cost-effective
  - Insufficient foundry volumes in specialized processes for narrow applications
- Reliability
  - Design/process specific issues
  - Temperature stability
  - Reliability validation difficult without acceleration mechanisms
- Control
  - High voltage or current requirements
  - Switching time slower than solid-state
  - Limited DC-RF isolation

Which MEMS-enabled Radio?

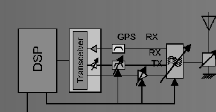
- Component Replacement
  - Performance



- Separate FDD and TDD Chains
  - Performance
  - Area
  - Cost
  - BOM



- Single Chain
  - Optimum
  - Requires fast tuning



- Sequence/Mixture of above or maybe something else entirely?!

Tunable vs. Reconfigurable

Continuously Tunable	Reconfigurable
Lower Element Precision	High Precision Required
Temperature Sensitive	Less Temperature Sensitive
Closed Loop Control Req.	Open Loop Possible
Lower Q's	Higher Q's
Fewer Elements	More Elements
RF Voltage Sensitivity	High Linearity
Variable Drive	Single Voltage Required
Analog Control	Digital Control

wiSpry Technology Platform

- High-performance *switchable* capacitors *integrated on …*
- 8" high-voltage CMOS supply/control *protected with …*
- Thin-film wafer level sealing *flip-chipped onto …*
- High Q integrated passive substrates *to create …*
- *Reconfigurable* RF components and modules

- Comprehensive integration roadmap
  - RFCMOS, SiGe, switches
- Addressing Broad Range of Market Applications
  - Extensive Reuse of Proven Components
  - Achieve Manufacturing Economies of Scale
- Stable predictable settings over temperature
- High DC-RF isolation
  - Dense packing of multiple devices
  - Series RF elements

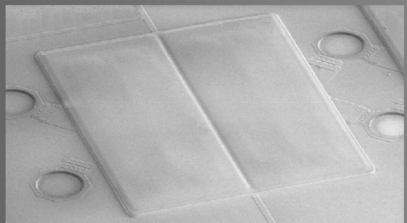
Thin-film Wafer-Level Encapsulation

Lower Cost
- Cavity packaging expensive
- Higher yield
- Standard backend processing for bumping, thinning and dicing

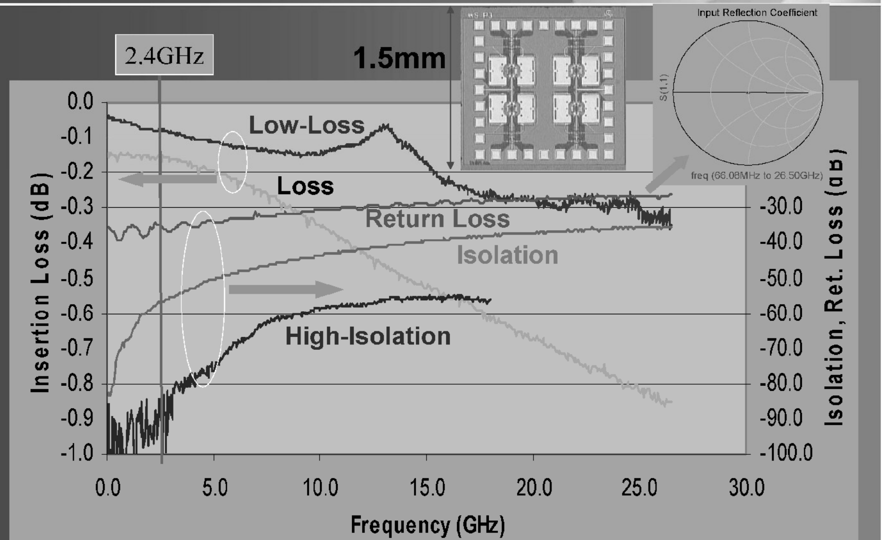
Easier Integration
- MCM
- Flip-chip
- Monolithic

Longer Life
- Sealed in fab clean room
- Controlled atmosphere

Higher Performance
- Controlled Impedance
- Chip-on-board, etc.

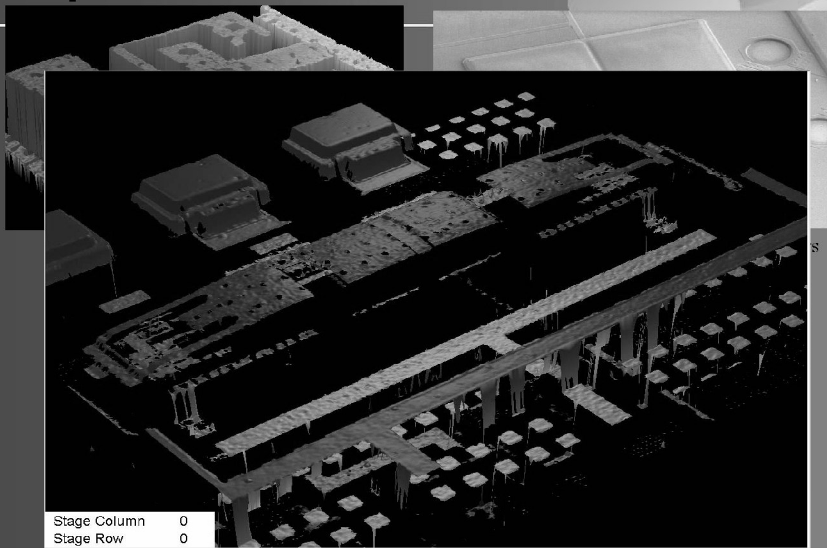


Switch Die S-parameters



Non-deembedded results!

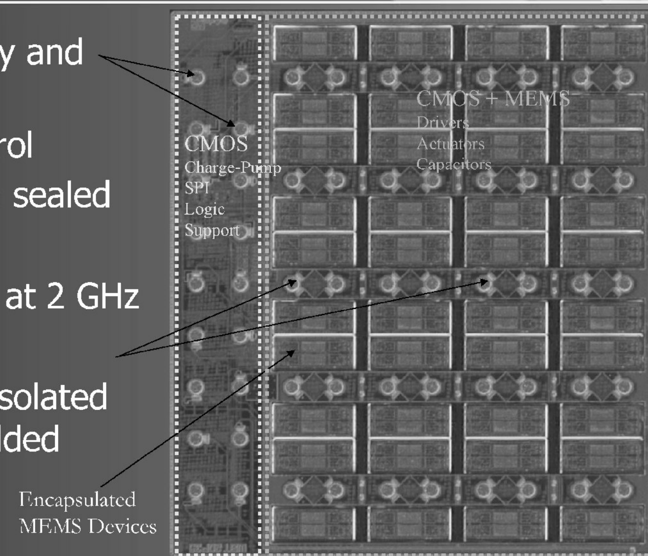
Capacitor with Thin Film Seal



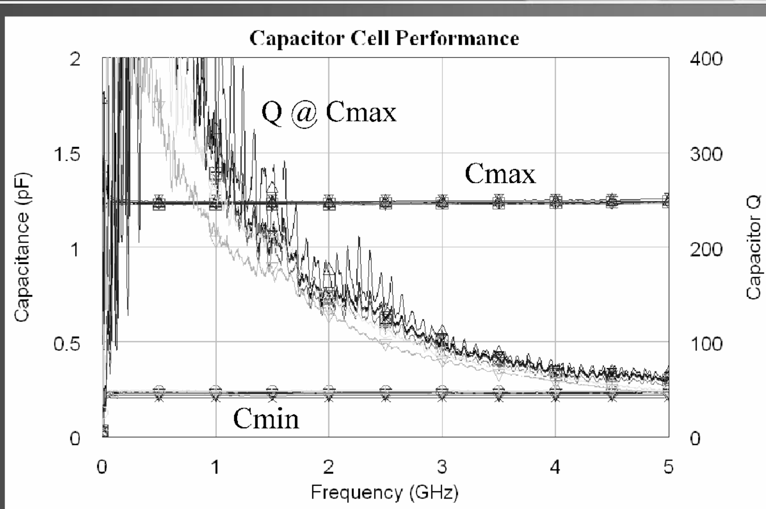
Actuated Wyko of Sealed MEMS on CMOS

Digital MEMS Capacitor Array Die

- 3V supply and interface
- SPI control
- Thin-film sealed
- 20pF
- Q > 100 at 2 GHz
- 7:1 ratio
- RF pins isolated and shielded
- Flip-chip



Unit Cell Performance

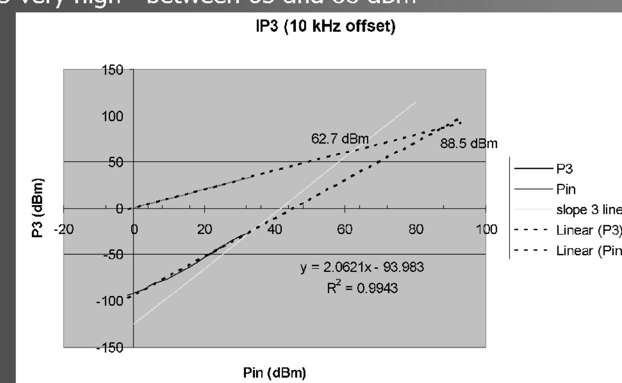


Non-deembedded results including all parasitics!

Linearity of Switched Capacitors

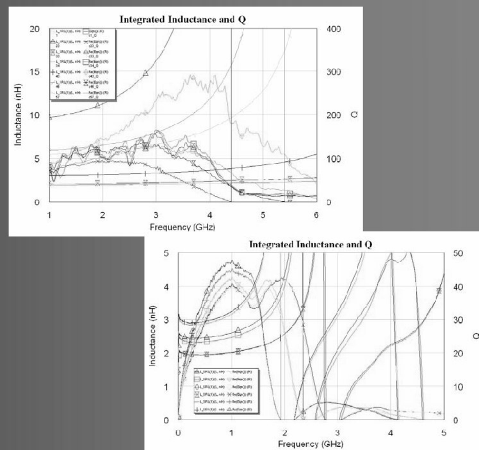
Two-tone measurements

- 10 kHz offset at 1 watt per tone
- Results at instrumentation limits
- IP3 very high - between 63 and 88 dBm



SIP Inductors

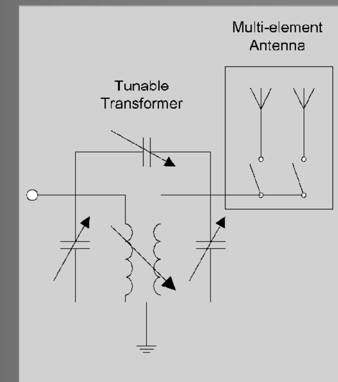
- Flip-chip tunable MEMS+CMOS onto multi-layer package containing high-Q fixed passives



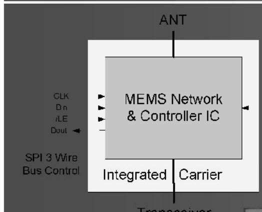
- Organic Substrate
  - L up to 10 nH
  - Q mostly > 100
  - SRF > 4 GHz
- Ceramic Substrate
  - L up to 5 nH
  - Q > 40
  - SRF > 2 GHz

Optimized Antenna Matching

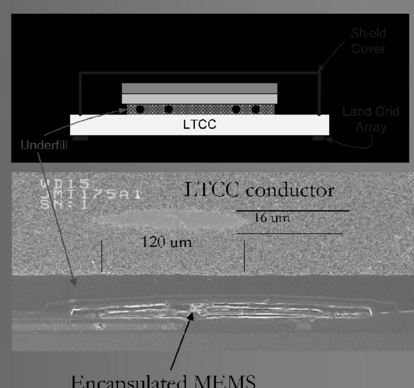
- 10% power reflection -> 0.5 dB loss
- Impedance variations
  - On metal surface – impedance / 2
  - Open/closed clamshell
  - Hand/Head position
  - In my pocket
  - Temperature swings
  - Manufacturing tolerances
- Band switching
  - Match shift and optimization
  - Reconfigurable antenna
- Rapid platform development and BOM reduction
- Use MEMS to implement tunable and switchable antenna



Impedance Matching Network



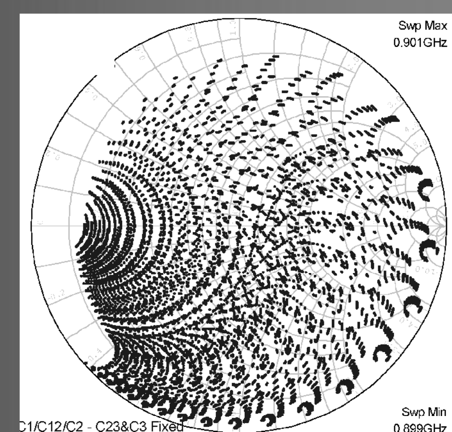
- Features
  - Operates from 3V supply (< 100 uA)
  - SPI Tune Control



- Assembly
  - 0.18 HV CMOS / MEMS die
  - LTCC Passives
  - Flip chip die to LTCC
  - Underfilled

Matching Network Circuit Design

- Specifications
  - 0.8-2.2 GHz
  - 5 Tuning MEMS Elements
  - 20 pF total capacitance
  - 10:1 ratio
  - 4-bit resolution shown at 900 MHz
  - 9:1 VSWR matched to 1.5:1
  - Loss 0.5 dB typ.



Tunable Antennas

- Low Loss and Highly Linear Tunable RF ICs Enable Antennas with:
  - Tunability over at least one octave
  - Sub-band Operation
    - Pre-select and spur suppression
  - Impact on Antenna Volume (space) & Efficiency by enabling:
    - Smaller Volume & Same Efficiency or
    - Same Volume & Higher Efficiency
  - Fairly Omni-directional Patterns
  - Well-Matched
    - VSWR < 1.5:1 over passband

Tunable Antenna Tradeoffs

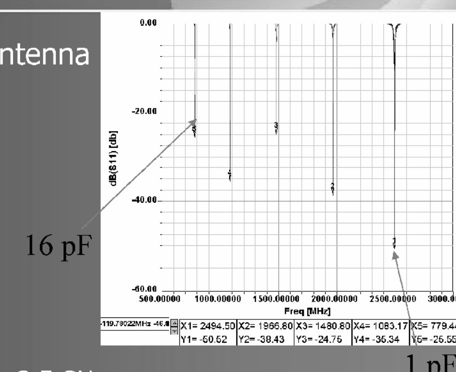
- Benefits
  - Smaller size
  - Reduced interference
  - Adaptive
  - Lower loss
  - Improved match
  - Higher sensitivity
  - Pattern breadth
  - Pattern stability
- Challenges
  - Precision
  - Stability
  - Control
  - Linearity
  - Cost
  - FDD instantaneous bandwidth
  - Multi-mode simultaneous operation
  - Tuning Speed

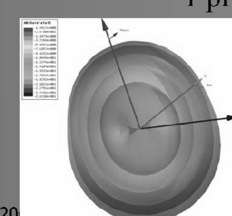
Performance of Small Antennas

- Chu-Harrington - Resonant bandwidth
  - Minimum $Q \approx \eta / (ka)^3$ for electrically small antenna
    - a is radius of sphere enclosing antenna
  - Multiple resonances required to expand bandwidth
    - Size and performance compromise
- Radiation Efficiency – Losses
  - Smaller antenna increases current density
  - High loading can double resistive losses
  - Tuning device finite Q further degrades efficiency
- Gain – Pattern Control
  - Radiation pattern simpler for small antennas

Tuned PCB Patch PIFA

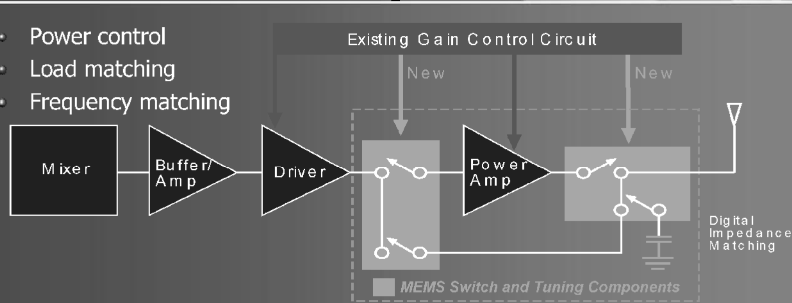
- PIFA – planar inverted F antenna
- 5mm x 10mm patch
- 62mil Rogers RO4350
  - 1.5 oz copper
- MEMS capacitor bank
  - Tunable from 1.0 – 16.0 pF
  - ESR < 0.1 ohm
  - SRF > 10 GHz
- > octave coverage
  - Center frequency from 0.8 – 2.5 GHz
  - Instantaneous BW from 0.38 – 5.8 MHz
  - Radiation efficiency w/ untuned feed - 10-57%
    - Limited by copper losses, not by capacitor Q
    - Antenna design improvement ongoing





Multi-Band and Dynamic Load PA

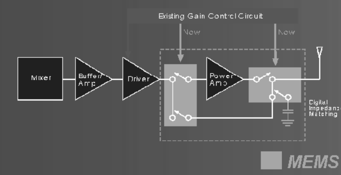
- Power control
- Load matching
- Frequency matching



- Optimum transistor load line at full power
  - $(3V)^2/2$ watts = 4.5 ohms
- Optimum transistor load line at 10% power
  - $(3V)^2/0.2$ watts = 45 ohms
- High Q MEMS to adjust output impedance and PA internal matching
  - Possibly separate harmonic adjustment
- Maintain efficiency near 50%!

Dynamic Load PA

Talk Time Extensions using Tunable load matching



Calculation demonstrating the effect of tunable load control for various output power levels.

	Vcc & Gain cntrl	Mems tunable	Vcc & Gain cntrl	Mems tunable	Vcc & Gain cntrl	Mems tunable
PA Power	28 dBm	28 dBm	24 dBm	24dBm	16 dBm	16 dBm
PAE	42%		30%		18%	
PAE mems		42%		35%		35%
Talktime	112 mins	112 mins	174 mins	189 mins	302 mins	345mins

680 mAh battery

Summary

- System Needs are Pressing
  - Additional Modes and Bands
  - More Spatial and Frequency Agility Requirements
  - Cost, Size and Power Constraints tighten
- RF-MEMS provides outstanding performance and agility
  - Optimum system implementation TBD
- Low cost overall solution is key
  - Wafer-level chip-scale packaging
  - True relay -> No off-chip components required for DC-RF **Isolation**
  - Multi-product Process that drives **Integration** and Aggregates **Volume**
- High reliability achieved
  - DFM Methodology Integrated with RF IC Flow
  - Proven to > 10^9 cycles
- Control issues resolved
  - Monolithic integration of generation and digital control interface
  - Speed sufficient for most commercial applications
- MEMS are ready for prime-time in RF front-ends!

Questions/comments:
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www.wispry.com